

Model Name: Z590 UD AC

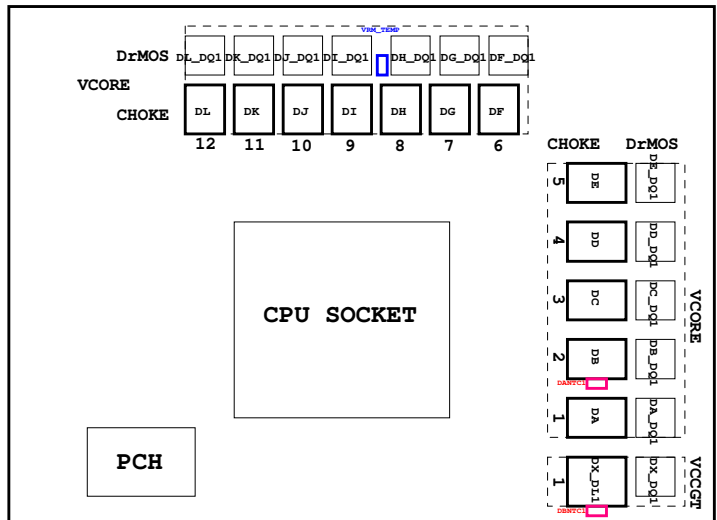
rev 1.01

SHEET	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1200-A (RKL_R0.12)
05	CPU_LGA1200-B-DDR4 (RKL_R0.12)
06	CPU_LGA1200-C (RKL_R0.12)
07	CPU_LGA1200-D (RKL_R0.12)
08	DDR 4 CHANNEL A (CML_R0.1)
09	DDR 4 CHANNEL B (CML_R0.1)
10	PCH CLK,DMI,CNVI (RKL_R0.15)
11	PCH SPI,USB (RKL_R0.15)
12	PCH PCIE,SATA (RKL_R0.15)
13	PCH ESPI,MISC (RKL_R0.15)
14	PCH GPP,HDA (RKL_R0.15)
15	PCH PWR,GND (RKL_R0.15)
16	Heatsink
17	ITE ITE8689 (RKL_R0.1)
18	HWM (RKL_R0.1)
19	FAN CTRL-CFL-SIO_5 FAN (RKL_R0.1)
20	Single BIOS for CS mode (RKL_R0.1)
21	PCI EXPRESS X16 SLOT (REV0.3)
22	PCI EXPRESS X4 SLOT (PCH) (REV0.51)
23	PCI EXPRESS X1 *3 (REV0.51)
24	SATA
25	M.2 x4 (A) (RKL_R0.1)
26	M.2 x2 (M) (RKL_R0.1)
27	M.2 x4 (P) (RKL_R0.1)
28	COM,LPT,TPM, THB (CML_R0.94)
29	ISL69269_L=0.15u (RKL_R0.1)
30	RAA229001_L=0.15u (RKL_R0.1)
31	VCORE_PSTAGE-1_L=0.15u (RKL_R0.1)
32	VCORE_PSTAGE-2_L=0.15u (RKL_R0.1)
33	VCORE_PSTAGE-3_L=0.15u (RKL_R0.1)
34	VCCGT_PSTAGE_L=0.15u (RKL_R0.1)
35	VCCSA_MOS (RKL_R0.1)
36	VCCIO-Ferrite-Z系列 (RKL_R0.2)
37	VCCIO2-Ferrite-Z系列 (RKL_R0.2)
38	RT8120_DDR_CHOKE-Ferrite-2L (RKL_R0.1)
39	RT8120_VPP_CHOKE-合金
40	NCP81269_VCC18_PCH
41	RT8068_VCC1V8_PRIM
42	DISCRETE POWER (REV0.1)
43	ATX POWER , A_-PROCHOT
44	DP PORT (RKL_R0.96)
45	CNVi_M2_WIFI (CML_R0.94)
46	Redriver_A_Type-A (RKL_R0.1)
47	R_USB30 (CML_R0.94)
48	GENESYS GL850S_1 (RKL_R0.1)
49	GENESYS GL850S_2 (RKL_R0.1)

SHEET

TITLE

50	F_USB20 (CML_R0.94)
51	F_U32 (CML_R0.94)
52	KB_MS_USB (CML_R0.94)
53	FRONT Type-C USB3.1 GEN2
54	REALTEK RTL8125BS (CML_R0.3)
55	U32_LAN CONNECTOR-8125 (CML_R0.3)
56	Realtek ALC897 (RKL_R6.0)
57	REAR AUDIO JACK (RKL_R6.0)
58	CPU POWER-1 (RKL_R0.11)
59	CPU POWER-1 (RKL_R0.11)
60	NCT3933 (RKL_R0.11)
61	F_PANEL
62	IT5702 (RKL_R1.0)
63	PCH/AUDIO/DEBUG/C_LED1/2 (RKL_R1.0)
64	D_LED1/D_LED2 (RKL_R1.0)
65	SMBUS SWITCH (RKL_R0.1)
66	CKG (RKL_R0.1)
67	EMI-ESD
68	POWER MAP
69	NTC MAP

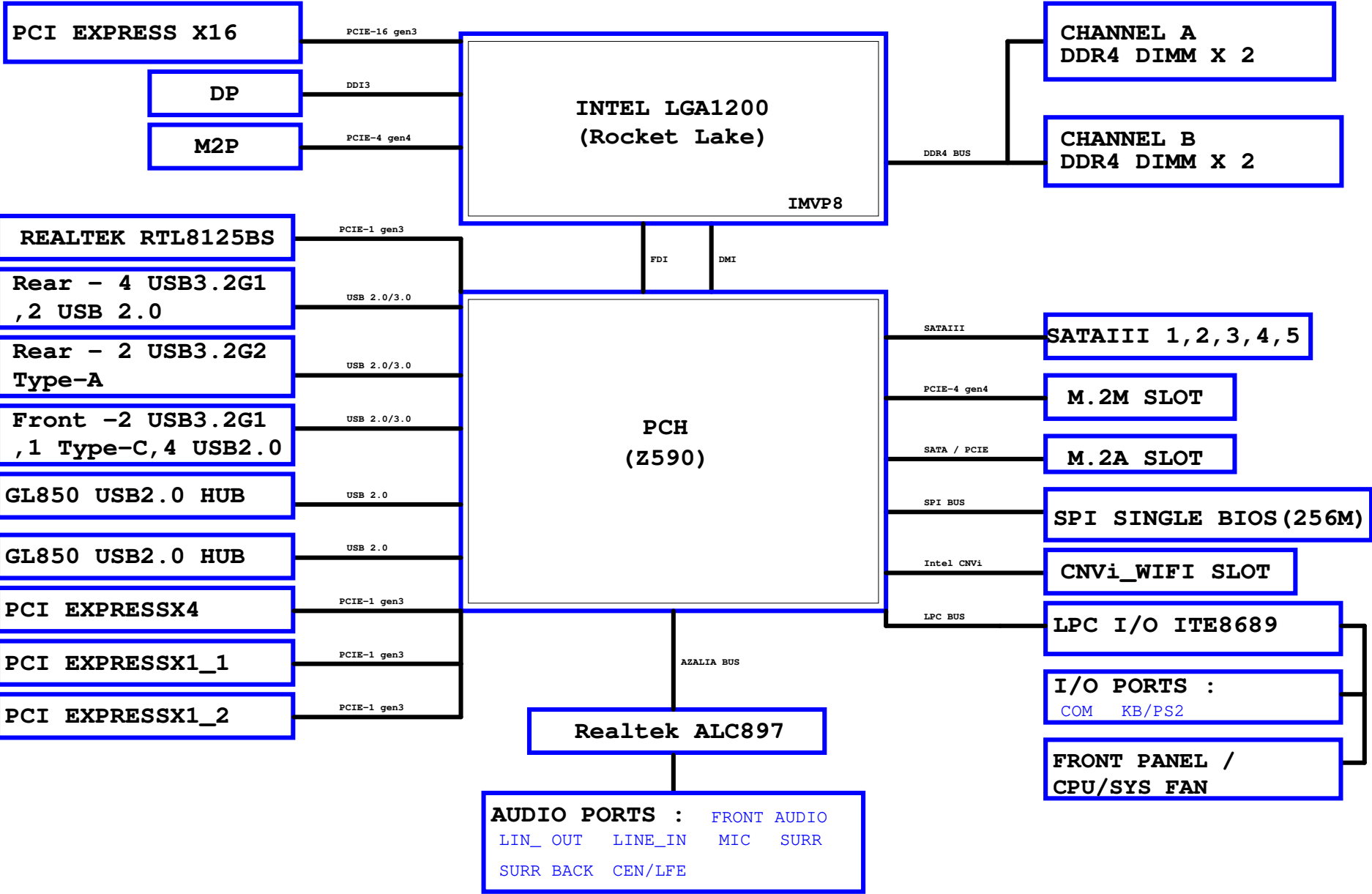


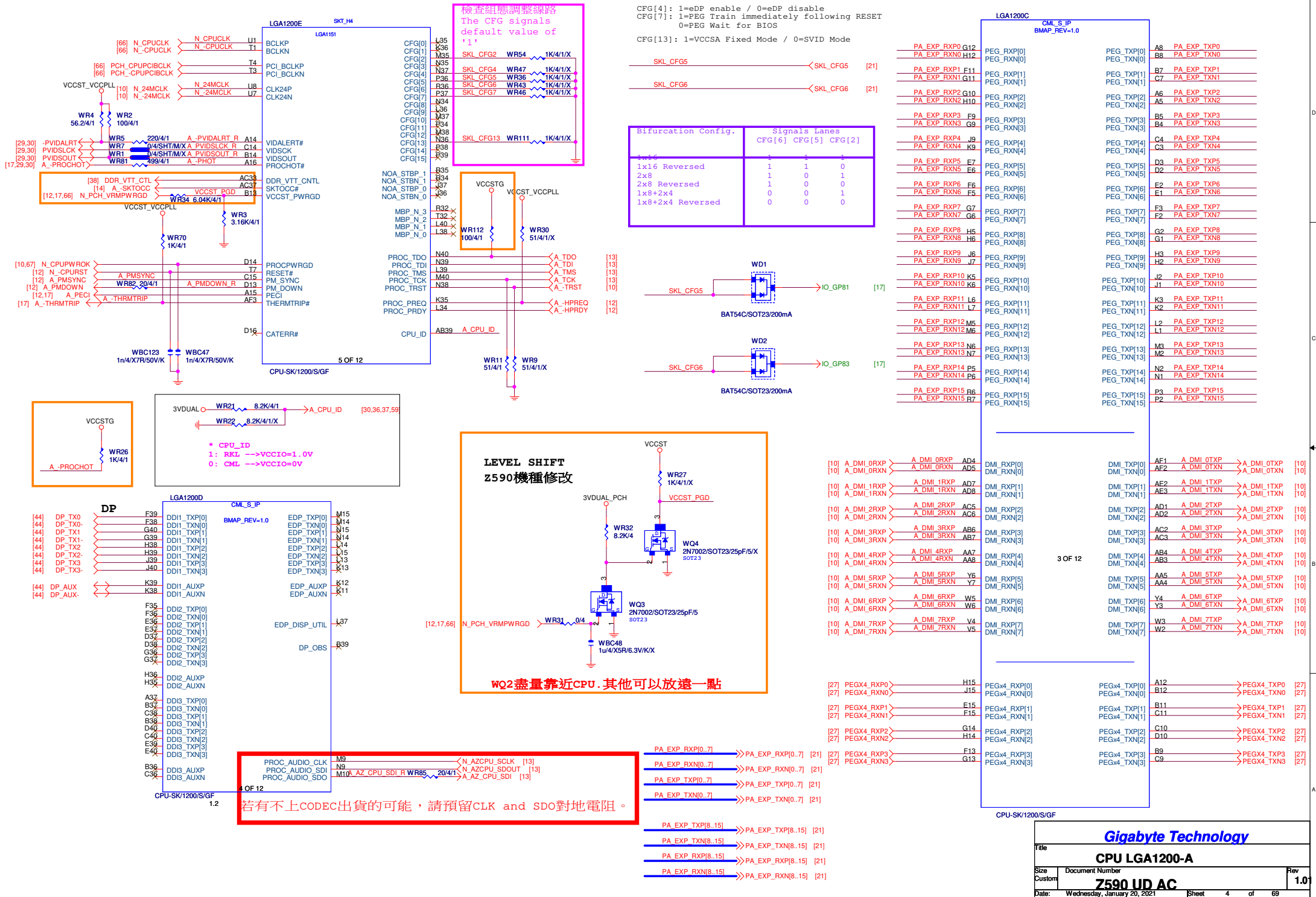
rev1.01 Circuit or PCB layout change

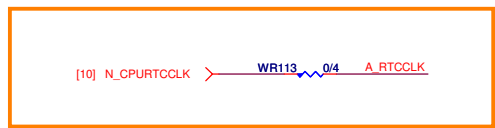
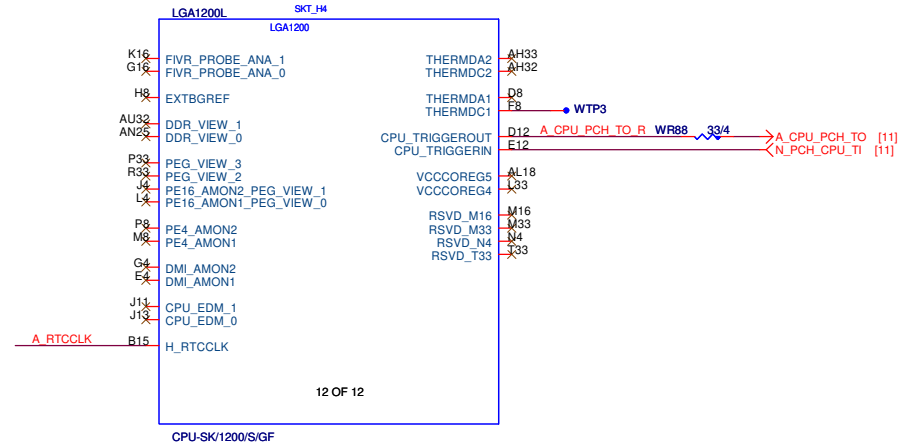
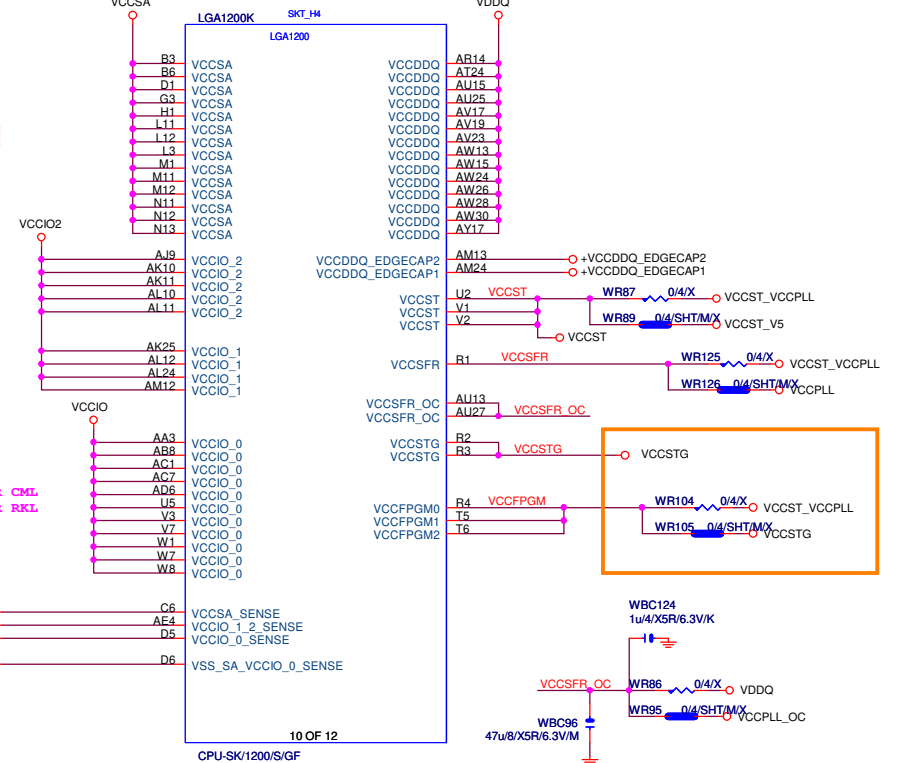
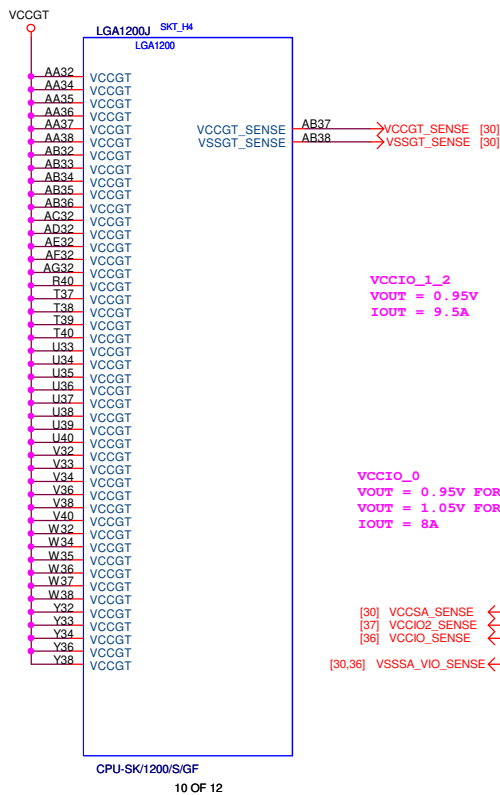
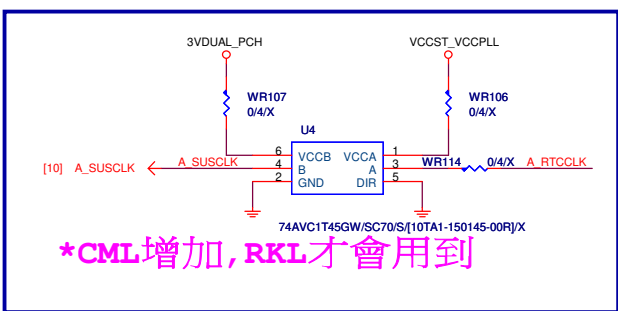
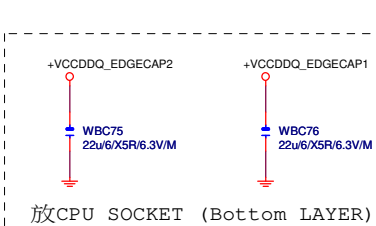
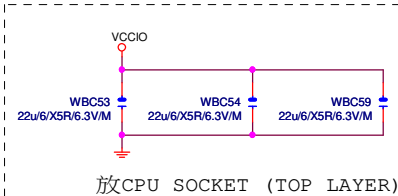
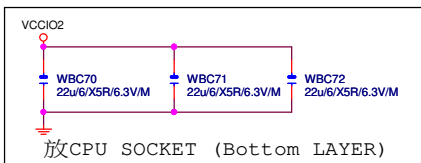
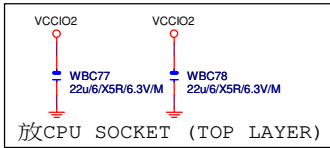
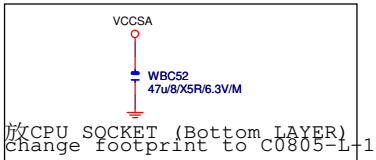
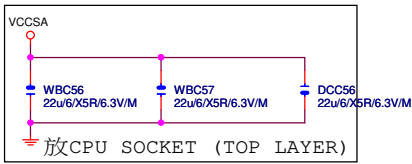
2017/07/19

[illegible]

BLOCK DIAGRAM







- [R] M00T_A0_3] < M00T_A0_3
- [R] M0A0_03] < M0A0_03
- [R] M0A0_01_16] < M0A0_01_16
- [R] M_D0A0_07] < M_D0A0_07
- [R] M_D0A0_07] < M_D0A0_07

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若Power source 端PWM IC
已有擺放, 則可刪除

DDR4 Decouple

若Power source 端PWM IC
已有擺放, 則可刪除

DDR4 Decouple

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DDR4 Decouple



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DDR4 Decouple

若Power source 端PWM IC
已有擺放, 則可刪除

DDR4	Capture Value
SOC series	DDR4/288/BK/VA/S/G15/4ROW/LONG
UD series	DDR4/288/BK/VA/D/G15/ONE LATCH/LONG
Gaming series	DDR4/288/BK/VA/D/G15/ONE LATCH/LONG
Gl.Sniper	DDR4/288/BK/VA/D/G15/ONE LATCH/LONG

Gigabyte Technology

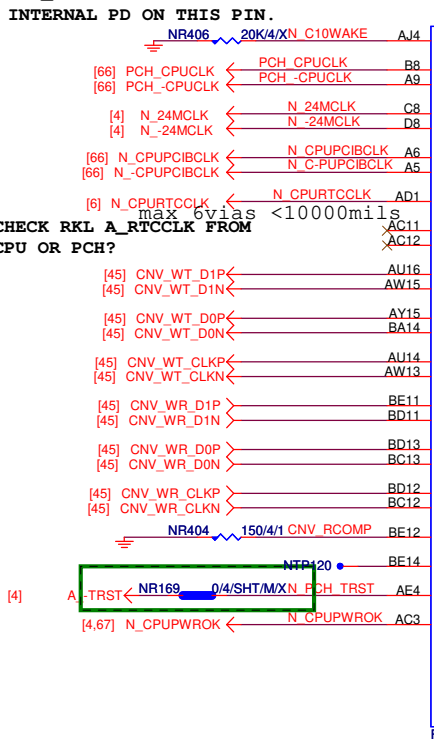
DDR4 CHANNEL A

Document Number: Z590 UD AC

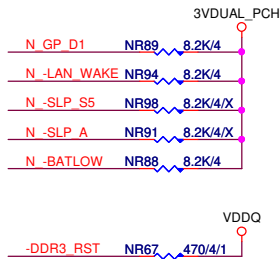
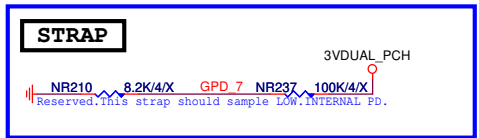
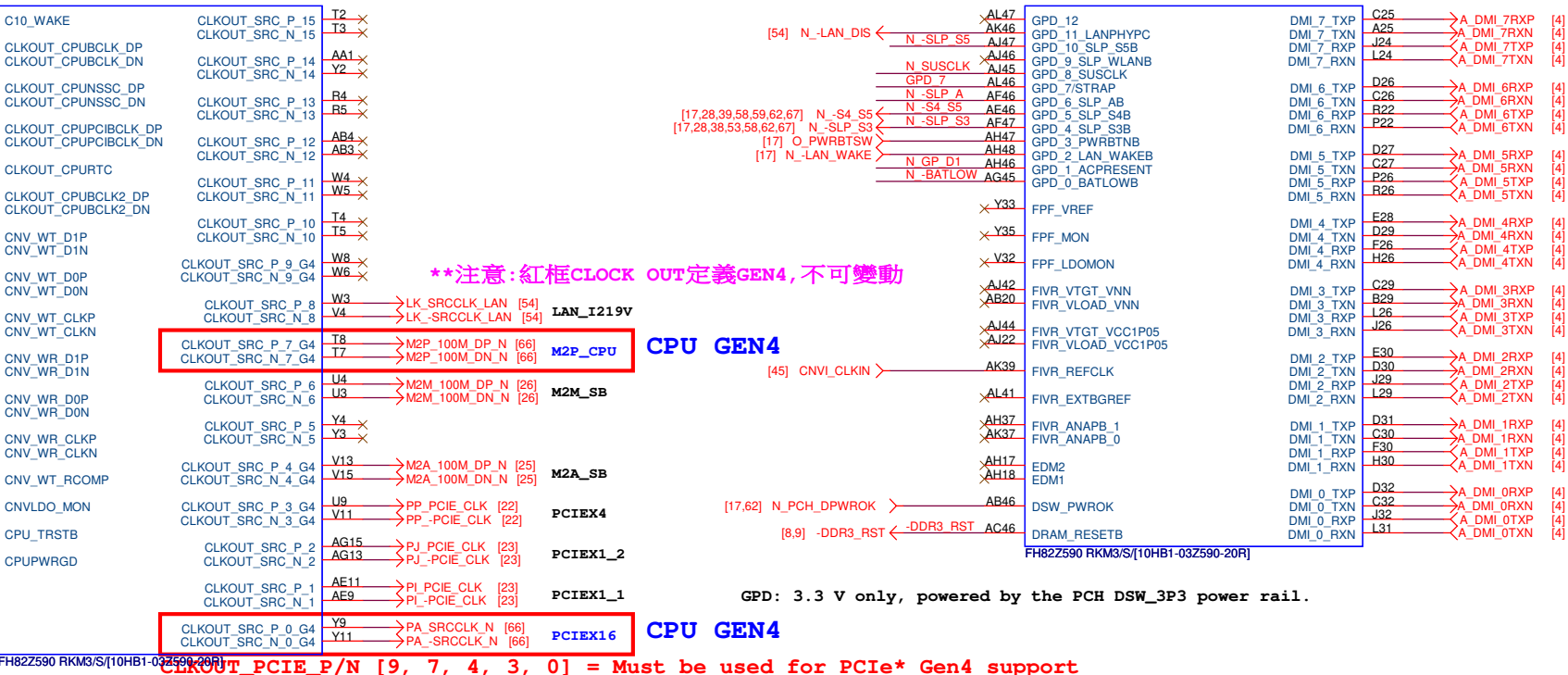
Rev: 1.01

RKL_TGP_PCH-H R0.15

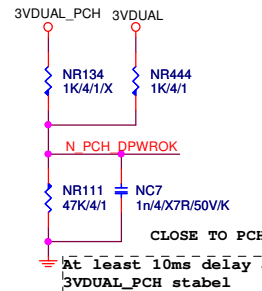
C10_WAKE RESERVED/BIOS NEED TO PROGRAM
INTERNAL PD ON THIS PIN.



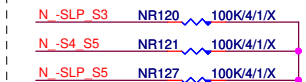
PCHB



N_SUSCLK MAX 2 LOADS SUPPORTED

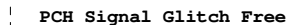


PCH Signal Glitch Free

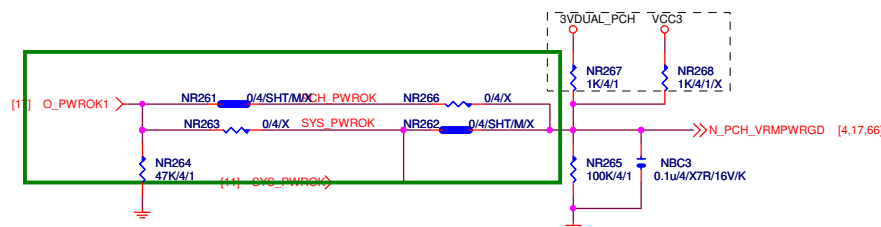
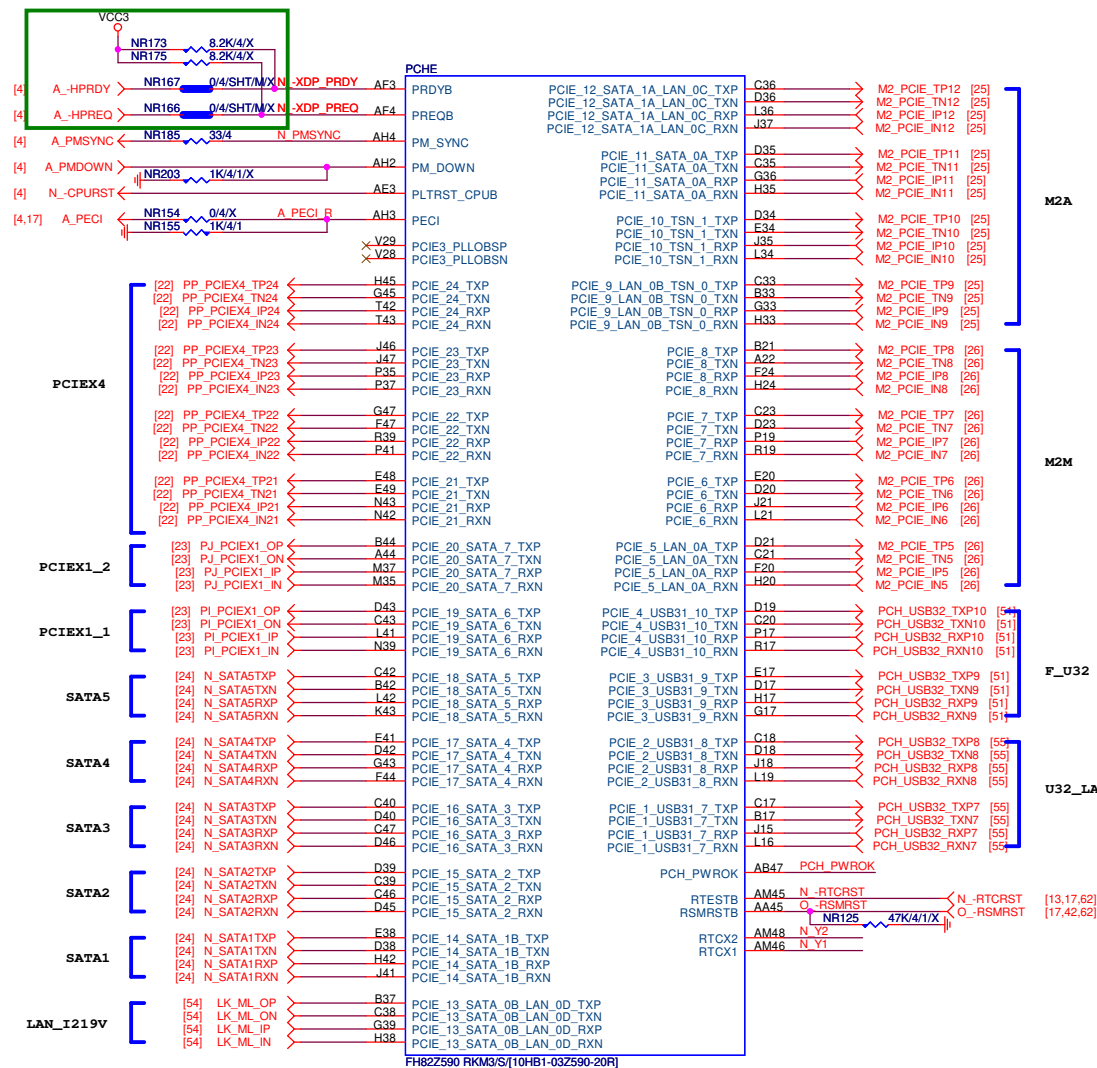


ANS	08656340	Gigabyte Technology
Title	PCH CLK,DMI,CNVI	
Size	Document Number	Rev
B	Z590 UD AC	1.0
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RKL_TGP_PCH-H R0.15

DC

RKL_TGP_PCH-H R0.15



Intel 500 series PCH PCIE P5-P12								
ITEM	PCIE P5	PCIE P6	PCIE P7	PCIE P8	PCIE P9	PCIE P10	PCIE P11	PCIE P12
H510	PCIE /GbE	PCIE	PCIE	PCIE	GbE ONLY	N/A	PCIE	PCIE /GbE
B560	PCIE /GbE	PCIE	PCIE	PCIE	PCIE /GbE	PCIE	PCIE SATA_0'	PCIE SATA_1' GbE
H570	PCIE /GbE	PCIE	PCIE	PCIE	PCIE /GbE	PCIE	PCIE SATA_0'	PCIE SATA_1' GbE
Z590	PCIE /GbE	PCIE	PCIE	PCIE	PCIE /GbE	PCIE	PCIE SATA_0'	PCIE SATA_1' GbE
Q570	PCIE /GbE	PCIE	PCIE	PCIE	PCIE /GbE	PCIE	PCIE SATA_0'	PCIE SATA_1' GbE
W580	PCIE /GbE	PCIE	PCIE	PCIE	PCIE /GbE	PCIE	PCIE SATA_0'	PCIE SATA_1' GbE
					Intel® RST for x2/x4 M.2			

Intel 500 series PCH PCIE P13-P24												
ITEM	PCIE P13	PCIE P14	PCIE P15	PCIE P16	PCIE P17	PCIE P18	PCIE P19	PCIE P20	PCIE P21	PCIE P22	PCIE P23	PCIE P24
H510	SATA_0 GbE	SATA_1	SATA_2	SATA_3	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
B560	SATA_0 GbE	SATA_1	SATA_2	SATA_3	SATA_4	SATA_5	N/A	N/A	PCIE	PCIE	PCIE	PCIE
H570	PCIE SATA_0 GbE	PCIE SATA_1	PCIE SATA_2	PCIE SATA_3	PCIE SATA_4	PCIE SATA_5	PCIE	PCIE	PCIE	PCIE	PCIE	PCIE
Z590	PCIE SATA_0 GbE	PCIE SATA_1	PCIE SATA_2	PCIE SATA_3	PCIE SATA_4	PCIE SATA_5	PCIE	PCIE	PCIE	PCIE	PCIE	PCIE
Q570	PCIE SATA_0 GbE	PCIE SATA_1	PCIE SATA_2	PCIE SATA_3	PCIE SATA_4	PCIE SATA_5	PCIE	PCIE	PCIE	PCIE	PCIE	PCIE
W580	PCIE SATA_0 GbE	PCIE SATA_1	PCIE SATA_2	PCIE SATA_3	PCIE SATA_4	PCIE SATA_5	PCIE SATA_6	PCIE SATA_7	PCIE	PCIE	PCIE	PCIE
					Intel® RST for x2/x4 M.2				Intel® RST for x2/x4 M.2			

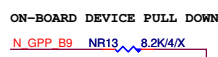
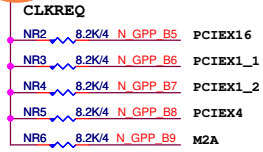
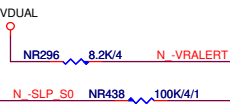
Intel 500 series PCH USB P7-P10				
ITEM	USB P7	USB P8	USB P9	USB P10
H510	NA	NA	NA	NA
B560	NA	NA	NA	NA
H570	U3.2 Gen1x1	U3.2 Gen1x1	PCIE	PCIE
Z590	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1
	PCIE	PCIE	PCIE	PCIE
Q570	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen1x1	U3.2 Gen1x1
	PCIE	PCIE	PCIE	PCIE
W580	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1
	PCIE	PCIE	PCIE	PCIE

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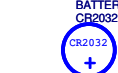
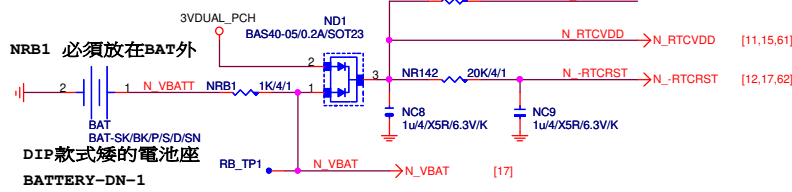
RKL_TGP_PCH-H R0.15

GPP_D PU/PD

GPP_B PU/PD



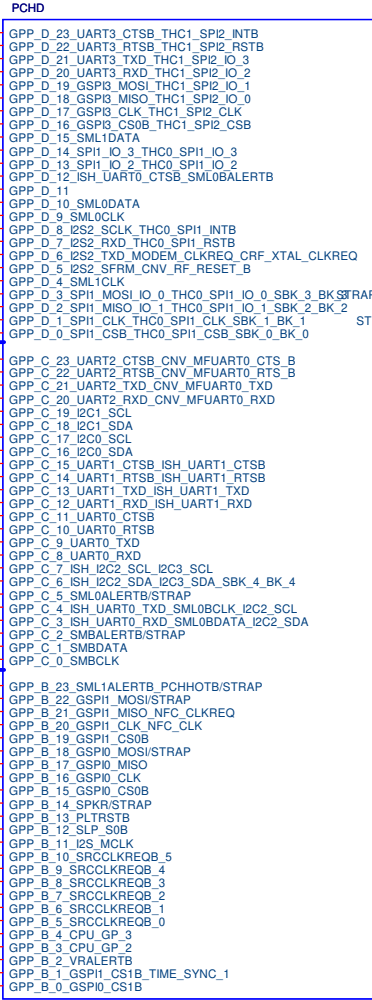
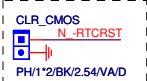
BATTERY



PCH Signal Glitch Free

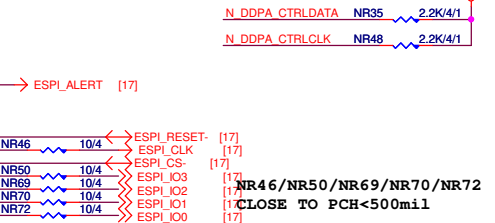
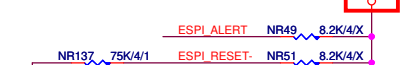
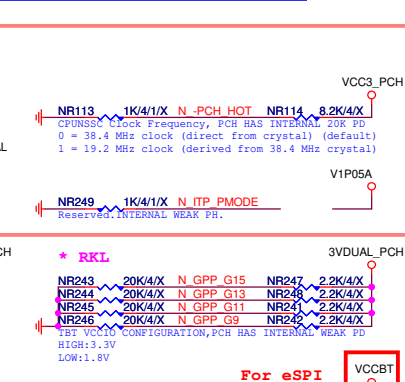
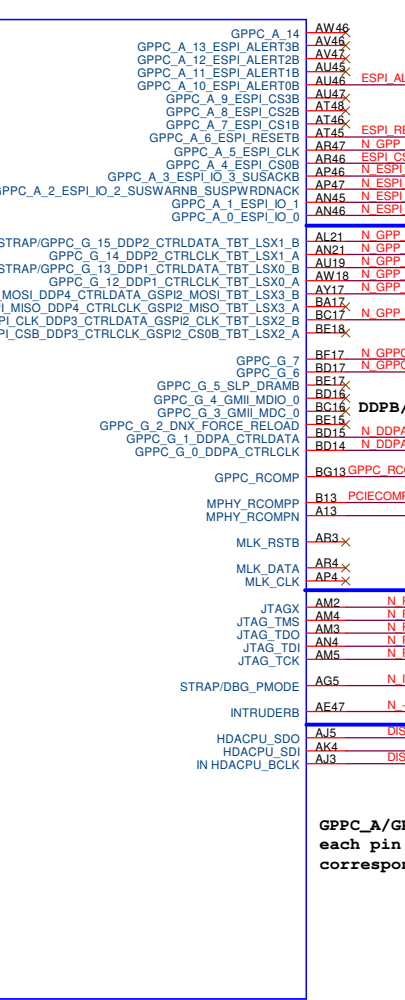
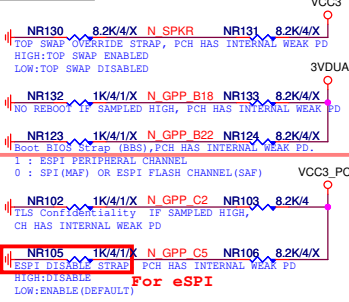


CLR_CMOS

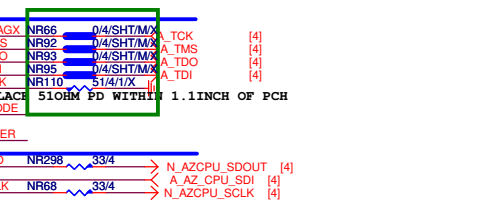
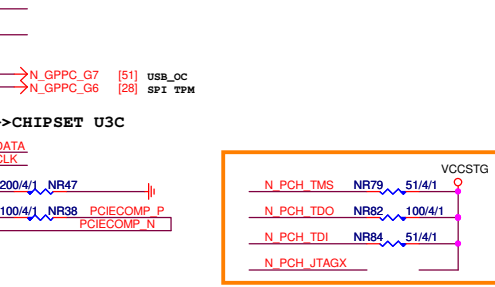


PH822590 RKM3/S(10HB1-03Z590-20R)

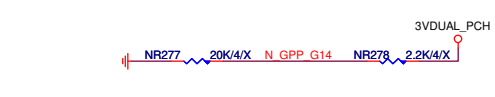
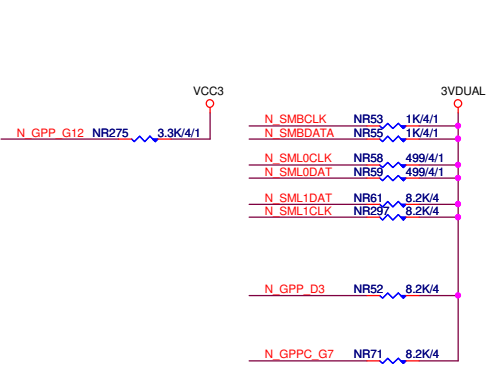
STRAP



TCP* pins can be routed to USB-C* connector or DP/HDMI native connector

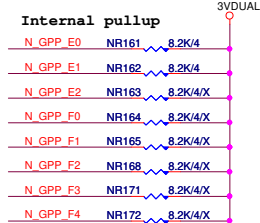
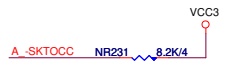
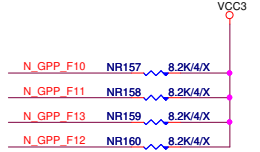
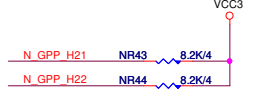
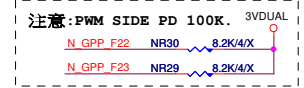
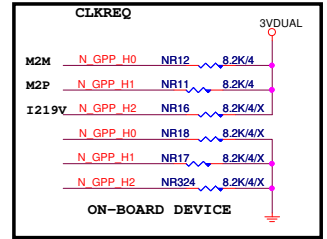


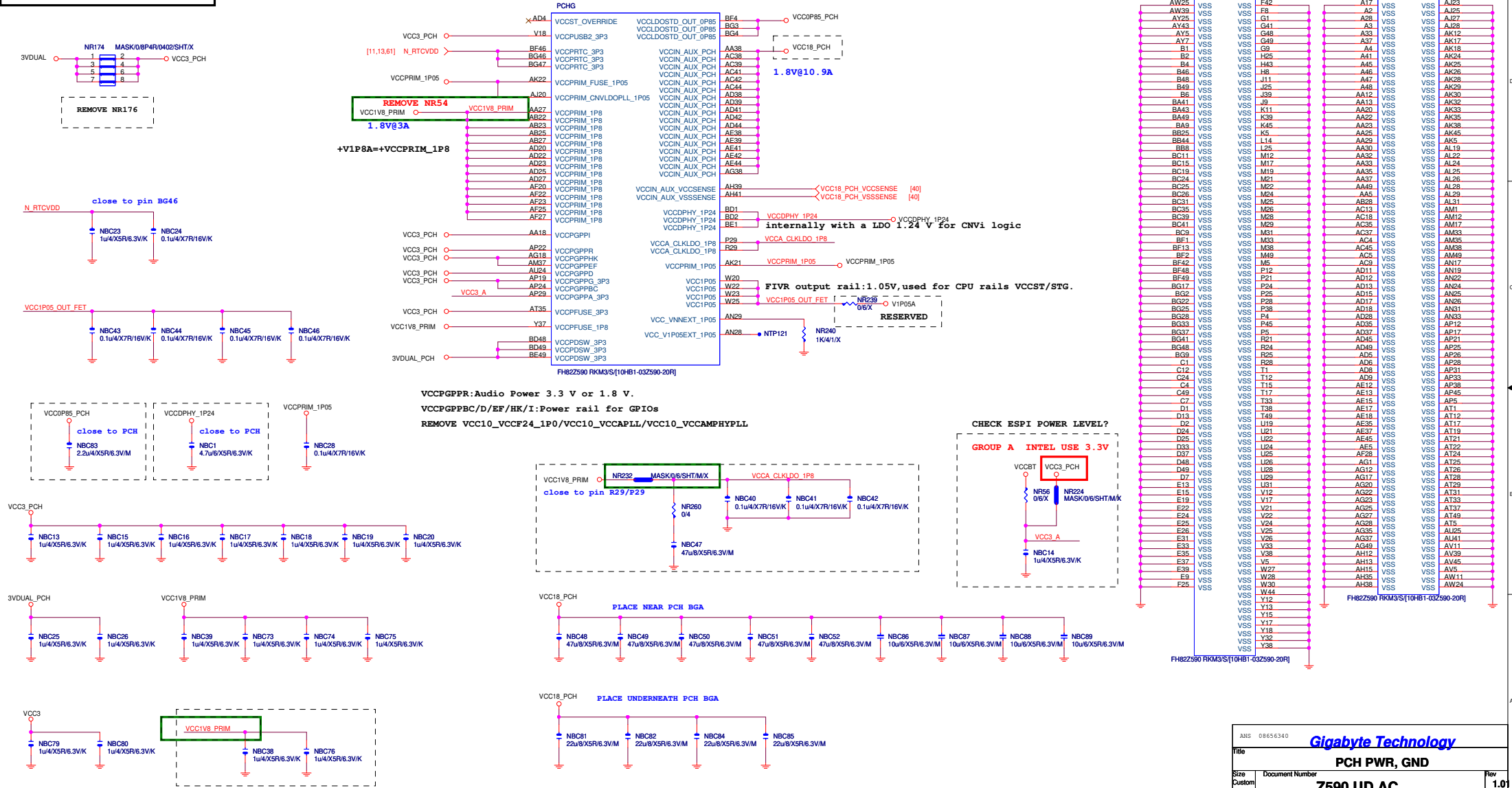
GPPC_A/GPPC_G (VCCPRIM_3P3 or VCCPRIM_1P8): each pin voltage is selected by setting the corresponding voltage select soft strap of the pin.



ANS 08656340		Gigabyte Technology	
Title		PCH ESPI, MISC	
Size	Document Number	Z590 UD AC	
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RKL_TGP_PCH-H R0.15





裝甲HEATSINK 分成四大部份

MOS_HS

Location: TMOS 12SP2-S09840-01R/02R/03R/04R
Location: RMOS 12SP2-S09423-11R/12R/13R/14R

TMOS
TMOS_Heatsink[12SP2-S09840-01R_12SP2-S09840-02R_12SP2-S09840-03R_12SP2-S09840-04R]

RMOS
RMOS_HS[12SP2-S09423-11R_12SP2-S09423-12R_12SP2-S09423-13R_12SP2-S09423-14R]

Footprint :
SINK_Z590_UD-AC-T

Footprint :
SINK_Z490_UD-R

PCH_HS

Location: PCH_HS 12SP2-S08604-21R/22R/23R/24R

PCH_HS

1X

X2

PCH_FS[12SP2-S08604-21R_12SP2-S08604-22R_12SP2-S08604-23R_12SP2-S08604-24R]

Footprint :
BGHSINK-Z370_HD3P

裝甲

Location: REAR_HS 12KRC-0H0047-11R

REAR_HS

1X

X2

HEAT SINK[12KRC-0H0047-11R]

Footprint :
Z490_UD_IO_COVER

後窗鐵片

Location: IO_SH
UD 11AIO-010061-12R
UD AC 11AIO-010061-02R

IO_SH

IO

IO[11AIO-010061-02R]

*UD與UD AC鐵片不同

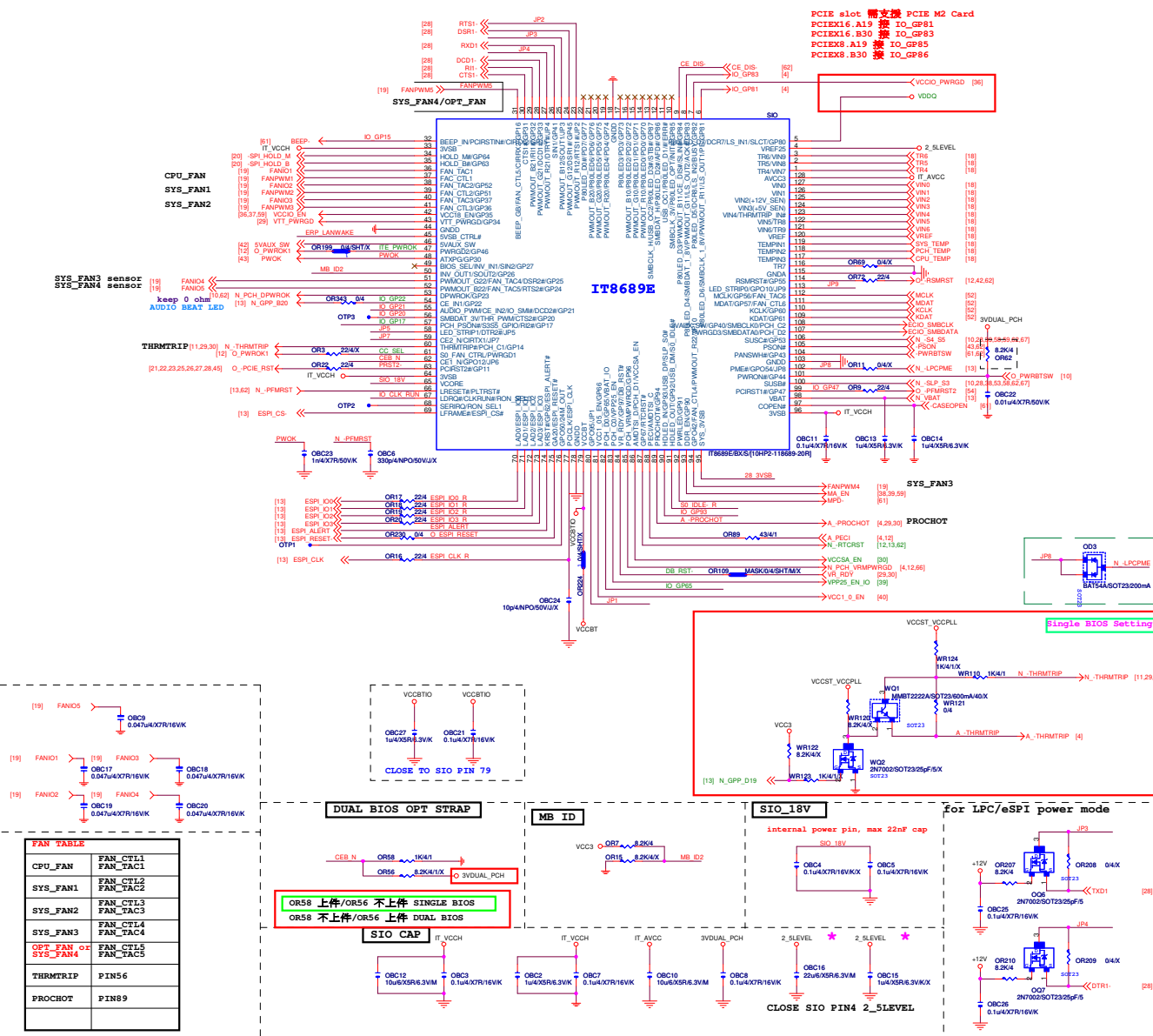
* PCB顏色 : 咖啡黑

* 文字面 : 灰色

* 疊構 : 2E7 (2OZ)

* 圖騰: ID設計Z590版GIGABYTE UD

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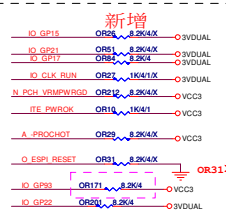
PWR_SHT



請依開案規格，選擇Support Exp下 LAN Wake up組態。

(組態一) PCIE LAN (Single & Dual LAN)

SIO_PU



(組態二) INTEL219 LAN (Single LAN)

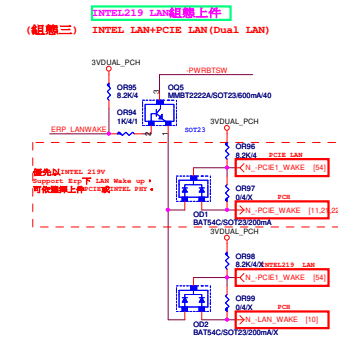
SIO_STRAP

SIO control detect

3V3V_PCH → OR47 1K4/1 → VDDQ

for eSPI

JP2	1	Disable WDT to rest PWRCK
JP3 <td>0<td>Enable WDT to rest PWRCK</td></td>	0 <td>Enable WDT to rest PWRCK</td>	Enable WDT to rest PWRCK
JP4 <td>1</td> <td>Dual-BIOS CS pin mode select bit '0'</td>	1	Dual-BIOS CS pin mode select bit '0'
JP5 <td>0</td> <td>LPCESPI power VCCBT = 3.3V</td>	0	LPCESPI power VCCBT = 3.3V
JP6 <td>1</td> <td>LPCESPI power VCCBT = 1.8V</td>	1	LPCESPI power VCCBT = 1.8V
JP7 <td>0</td> <td>ESPI I/F</td>	0	ESPI I/F
JP7 <td>1</td> <td>Enable Dual BIOS Function (for GigaByte Only)</td>	1	Enable Dual BIOS Function (for GigaByte Only)
JP3 <td>0</td> <td>Disable Dual BIOS Function (for GigaByte Only)</td>	0	Disable Dual BIOS Function (for GigaByte Only)
JP7 <td>1</td> <td>Dual-BIOS CE pin mode select bit '1'</td>	1	Dual-BIOS CE pin mode select bit '1'
JP7 <td>0</td> <td>CE pin disable (Hold pin mode)</td>	0	CE pin disable (Hold pin mode)
JP3 <td>0</td> <td>CE mode 1</td>	0	CE mode 1
JP3 <td>1</td> <td>CE mode 2</td>	1	CE mode 2
JP3 <td>0</td> <td>CE mode 3</td>	0	CE mode 3



ERP Wake on LAN		
Single LAN	Realtek	組態一
	Atheros	組態二
Dual LAN (只留一欄 LAN 交換器 ERP 下 WAKE UP)	Intel 219	組態一
	Atheros+Realtek	組態二
No Support ERP	Intel 219+Intel 210	組態三

VREF ←

7] SYS_TEMP ←

7] CPU_TEMP ←

7] PCH_TEMP ←

OC7 1u4/4XSR6.3V/K

OC8 1u4/4XSR6.3V/K

OR73 10K/4/1

R674 8.2K/4

R675 10K/4/1

SYS_TEMP1 10K/14/S

PCH_TEMP1 10K/14/S

Close S10

CLOSE PCH

[17] VREF

[17] TR4

[17] TR5

[17] TR6

OC17
1u4/X5R/6.3V/K

X16_TEMP1
10K/1/4/S

OC14
1u4/X5R/6.3V/K

VRM_TEMP
100K/1/4/S

OC15
1u4/X5R/6.3V/K

SYS_TEMP2
10K/1/4/S

CLOSE VCORE
MOSFET

OR211
10K/4/1

OR83
10K/4/1

OR85
10K/4/1

[illegible][illegible]

VCC_SIO

OR82

0/4/SHT/X

Rev:0.6

FOR EMI ONLY

+12V

C3
1n4/X7R/50V/

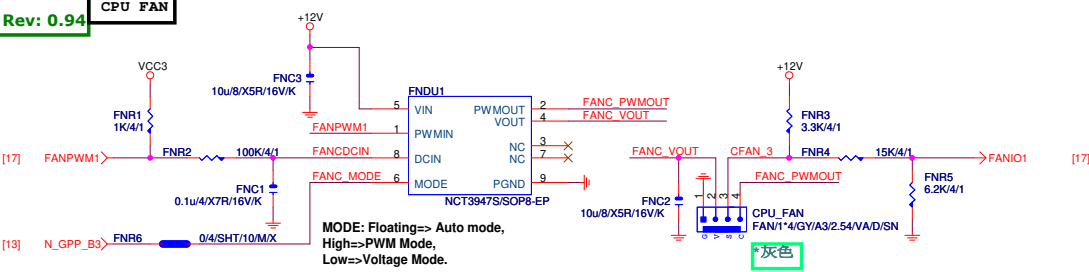
FOR EMI ONLY

VCC3

C2
0.1u/4/X7R/16V/

★Update 2015-04.24

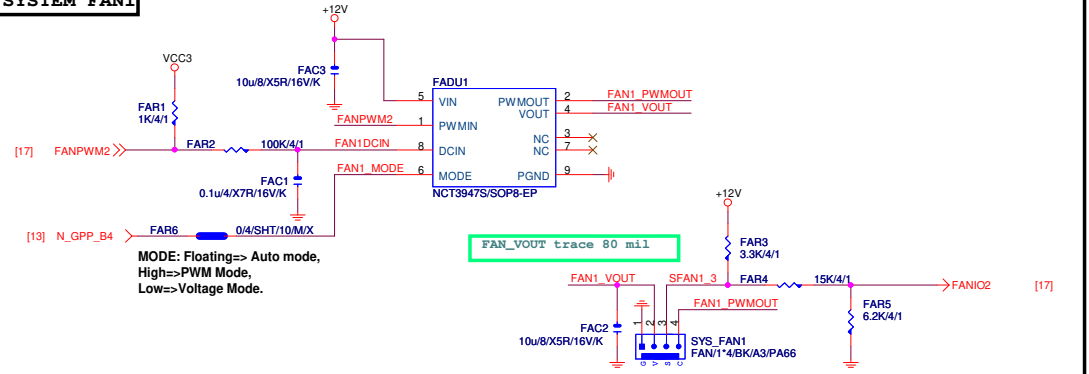
CPU_FAN



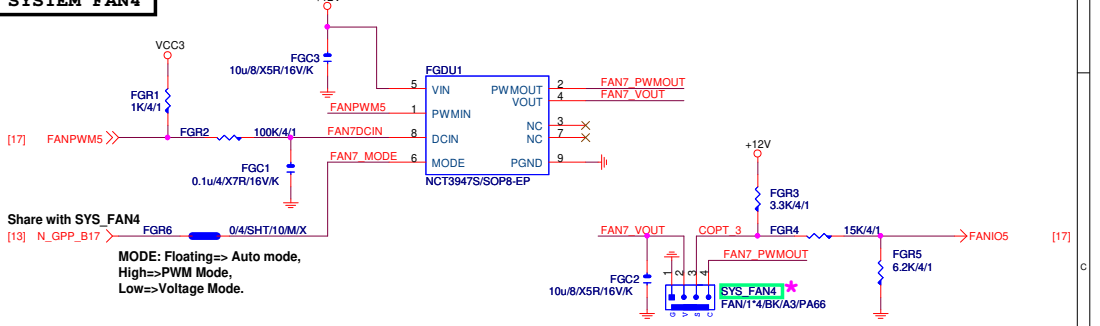
IO 4_FAN

- CPU_FAN
- SYS_FAN1
- SYS_FAN2
- SYS_FAN3
- SYS_FAN4

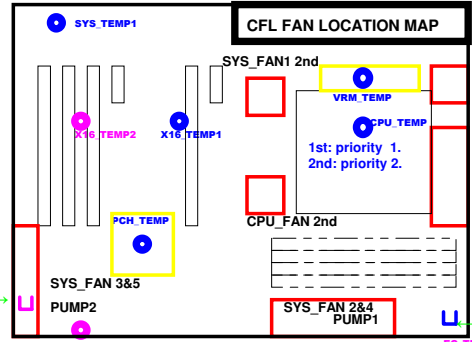
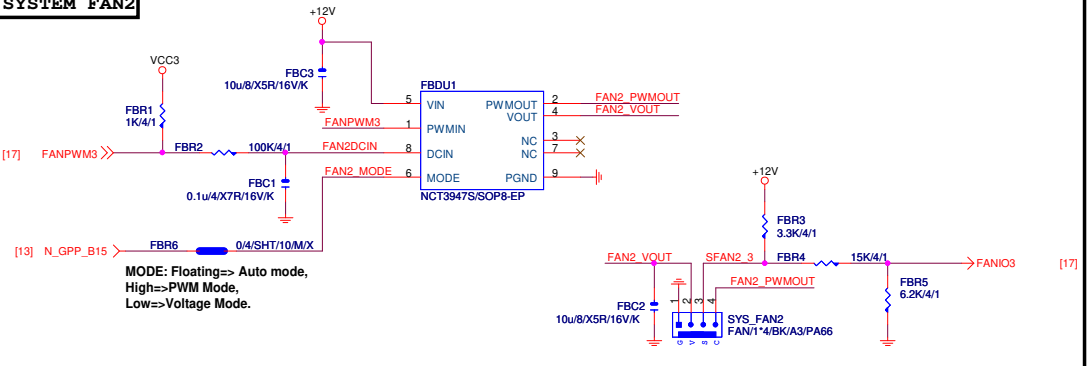
SYSTEM FAN1



SYSTEM FAN4

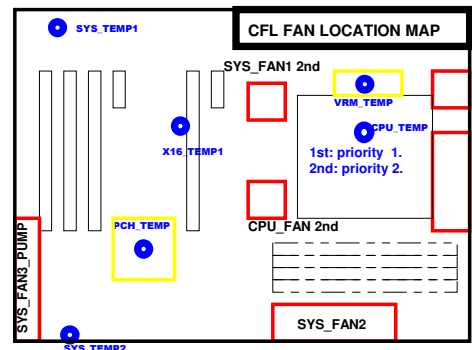
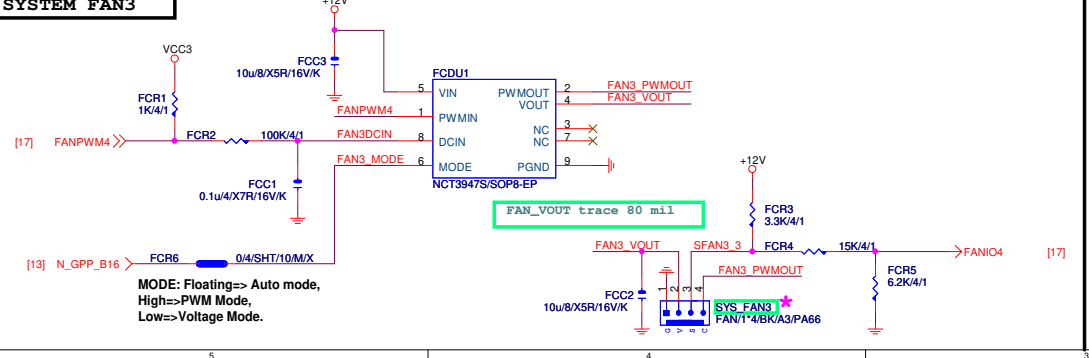


SYSTEM FAN2



- 8 FAN from IO & EC
- EC TEMP SENSE 879X
- IO TEMP SENSE 8686

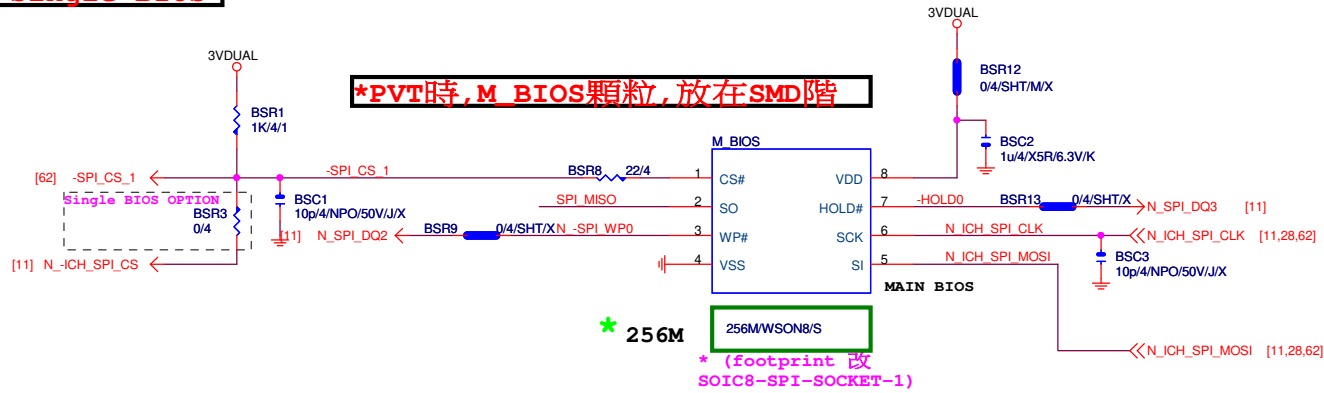
SYSTEM FAN3



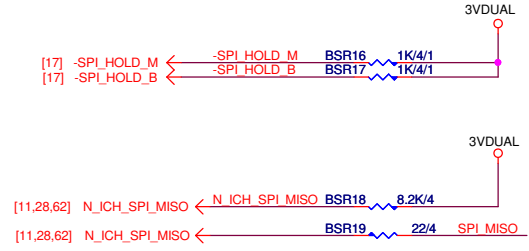
- 5 FAN from IO
- IO TEMP SENSE 8686

DUAL BIOS

***Single BIOS**

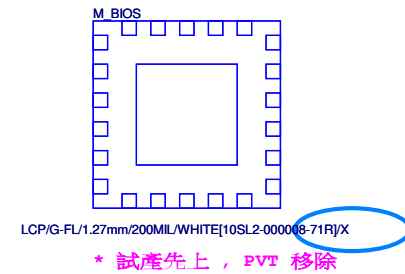


MOSI For DMI RX Termination Voltage



BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

1 means floating
0 means PD 1K



Rev 0.3

PCIEX16 CAP

PCIEX16 SLOT

PCIESLOT-1645TH

FOR SMBUS

PCIEX16不能short pad

[22,23,65] SMB_SW_SC1

[22,23,65] SMB_SW_SD

[11,17,22,23] N_PCIE_WAKE

-PCIEX16_PR

PA_EXP_TXP0_C

PA_EXP_TXN0_C

[13] -PCIEX16_PR

PA_EXP_TXP1_C

PA_EXP_TXN1_C

PA_EXP_TXP2_C

PA_EXP_TXN2_C

PA_EXP_TXP3_C

PA_EXP_TXN3_C

-PCIEX16_PR

PA_EXP_TXP4_C

PA_EXP_TXN4_C

PA_EXP_TXP5_C

PA_EXP_TXN5_C

PA_EXP_TXP6_C

PA_EXP_TXN6_C

PA_EXP_TXP7_C

PA_EXP_TXN7_C

-PCIEX16_PR

PA_EXP_TXP8_C

PA_EXP_TXN8_C

PA_EXP_TXP9_C

PA_EXP_TXN9_C

PA_EXP_TXP10_C

PA_EXP_TXN10_C

PA_EXP_TXP11_C

PA_EXP_TXN11_C

PA_EXP_TXP12_C

PA_EXP_TXN12_C

PA_EXP_TXP13_C

PA_EXP_TXN13_C

PA_EXP_TXP14_C

PA_EXP_TXN14_C

PA_EXP_TXP15_C

PA_EXP_TXN15_C

-PCIEX16_PR

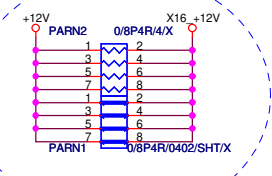
3GIO_*16

KEY

PCI-E16X-164P/BK/LONG DOUBLE/HK*2/SHELL/GEN4.0

黑色金屬加強

PCIEX16 PROTECT SHT

+12 protect
short-wire test

PCIEX16 AC CAP

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PA_EXP_TXP0	PAC5	0.22u4/X5R/6.3V/K	PA_EXP_TXP0_C
PA_EXP_TXN0	PAC4	0.22u4/X5R/6.3V/K	PA_EXP_TXN0_C
PA_EXP_TXP1	PAC6	0.22u4/X5R/6.3V/K	PA_EXP_TXP1_C
PA_EXP_TXN1	PAC7	0.22u4/X5R/6.3V/K	PA_EXP_TXN1_C
PA_EXP_TXP2	PAC8	0.22u4/X5R/6.3V/K	PA_EXP_TXP2_C
PA_EXP_TXN2	PAC9	0.22u4/X5R/6.3V/K	PA_EXP_TXN2_C
PA_EXP_TXP3	PAC10	0.22u4/X5R/6.3V/K	PA_EXP_TXP3_C
PA_EXP_TXN3	PAC11	0.22u4/X5R/6.3V/K	PA_EXP_TXN3_C
PA_EXP_TXP4	PAC12	0.22u4/X5R/6.3V/K	PA_EXP_TXP4_C
PA_EXP_TXN4	PAC13	0.22u4/X5R/6.3V/K	PA_EXP_TXN4_C
PA_EXP_TXP5	PAC14	0.22u4/X5R/6.3V/K	PA_EXP_TXP5_C
PA_EXP_TXN5	PAC15	0.22u4/X5R/6.3V/K	PA_EXP_TXN5_C
PA_EXP_TXP6	PAC16	0.22u4/X5R/6.3V/K	PA_EXP_TXP6_C
PA_EXP_TXN6	PAC17	0.22u4/X5R/6.3V/K	PA_EXP_TXN6_C
PA_EXP_TXP7	PAC18	0.22u4/X5R/6.3V/K	PA_EXP_TXP7_C
PA_EXP_TXN7	PAC19	0.22u4/X5R/6.3V/K	PA_EXP_TXN7_C
PA_EXP_TXP8	PAC20	0.22u4/X5R/6.3V/K	PA_EXP_TXP8_C
PA_EXP_TXN8	PAC21	0.22u4/X5R/6.3V/K	PA_EXP_TXN8_C
PA_EXP_TXP9	PAC22	0.22u4/X5R/6.3V/K	PA_EXP_TXP9_C
PA_EXP_TXN9	PAC23	0.22u4/X5R/6.3V/K	PA_EXP_TXN9_C
PA_EXP_TXP10	PAC24	0.22u4/X5R/6.3V/K	PA_EXP_TXP10_C
PA_EXP_TXN10	PAC25	0.22u4/X5R/6.3V/K	PA_EXP_TXN10_C
PA_EXP_TXP11	PAC26	0.22u4/X5R/6.3V/K	PA_EXP_TXP11_C
PA_EXP_TXN11	PAC27	0.22u4/X5R/6.3V/K	PA_EXP_TXN11_C
PA_EXP_TXP12	PAC28	0.22u4/X5R/6.3V/K	PA_EXP_TXP12_C
PA_EXP_TXN12	PAC29	0.22u4/X5R/6.3V/K	PA_EXP_TXN12_C
PA_EXP_TXP13	PAC30	0.22u4/X5R/6.3V/K	PA_EXP_TXP13_C
PA_EXP_TXN13	PAC31	0.22u4/X5R/6.3V/K	PA_EXP_TXN13_C
PA_EXP_TXP14	PAC32	0.22u4/X5R/6.3V/K	PA_EXP_TXP14_C
PA_EXP_TXN14	PAC33	0.22u4/X5R/6.3V/K	PA_EXP_TXN14_C
PA_EXP_TXP15	PAC34	0.22u4/X5R/6.3V/K	PA_EXP_TXP15_C
PA_EXP_TXN15	PAC35	0.22u4/X5R/6.3V/K	PA_EXP_TXN15_C

PCI-E REV:1.1--> 2.5GHZ

PCE-E X1(單向) BANDWIDTH=2.5GHz*(8b/10b)=2Gb/s=250MB/s

PCE-E X1(雙向) BANDWIDTH=2.5GHz*(8b/10b) X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWIDTH=2.5GHz*(8b/10b) X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWIDTH=2.5GHz*(8b/10b) X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--> 5GHZ

PCE-E X1(單向) BANDWIDTH=5GHz*(8b/10b)=4Gb/s=500MB/s

PCI-E REV:3.0--> 8GHZ

PCE-E X1(單向) BANDWIDTH=8GHz*(128b/130b)=8Gb/s=1GB/s

Gigabyte Technology			
Title			
PCI EXPRESS * 16			
Size	Document Number	Rev	
Custom	Z590 UD AC	1.01	
Date:	Wednesday, December 30, 2020	Sheet	21 of 69

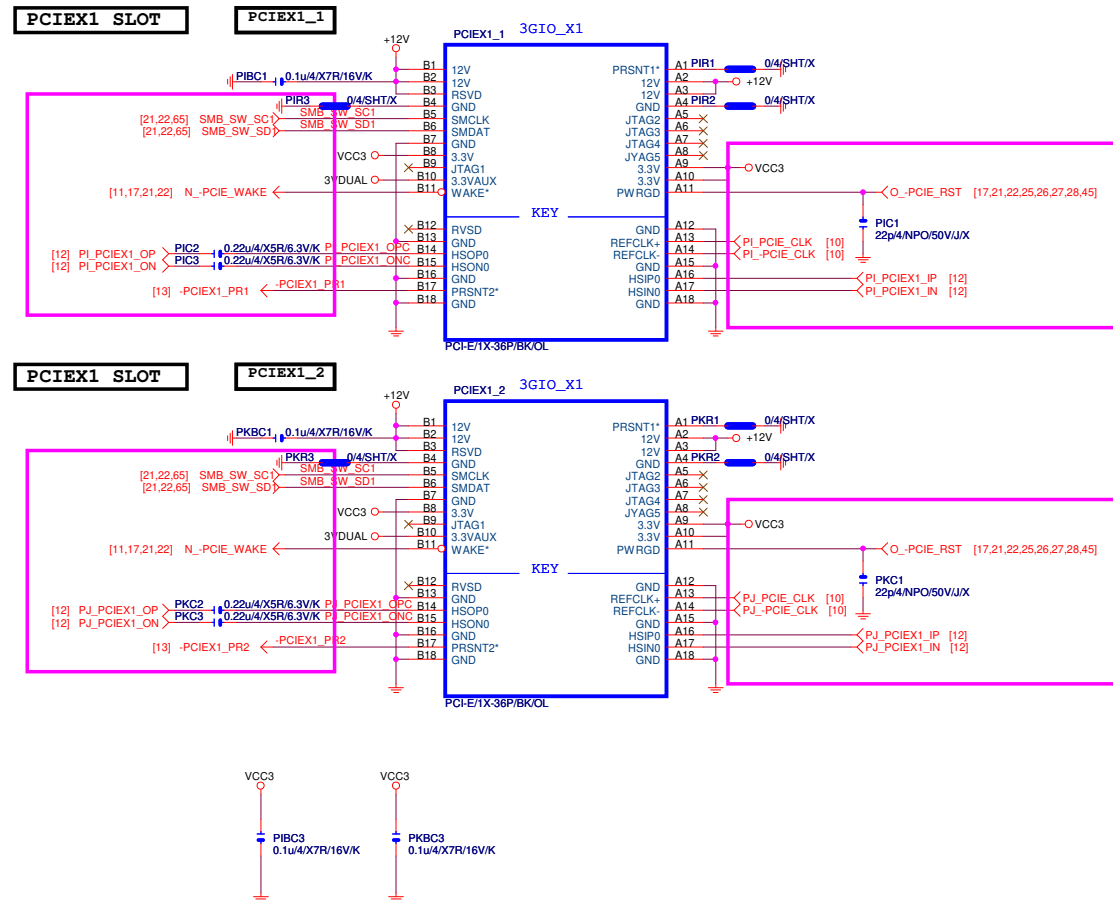
*
Footprint "PCIESLOT-64P-1"

PCIEX4 SM Bus電阻layout 改0 ohm
上件



Title			
PCIE X4			
Size Custom	Document Number		Rev
	Z590 UD AC		1.0
Date:	Wednesday, December 30, 2020	Sheet	22 of 69

Rev 0.51



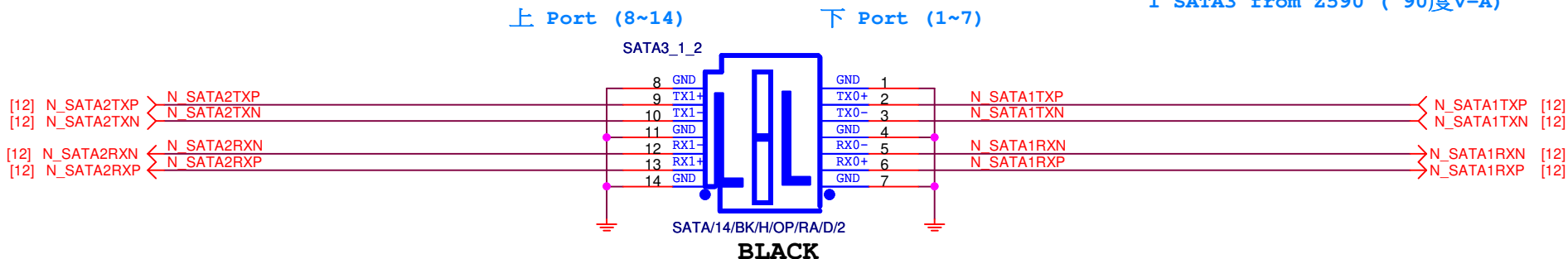
Gigabyte Technology			
Title			
PCIE X1 *3			
Size	Document Number	Rev	
Custom	Z590 UD AC	1.01	
Date:	Wednesday, December 30, 2020	Sheet	23 of 69

SATA3 1/2

IO19/IO20 To SATA3 port1/2

4 SATA3 from Z590 (180度R-A)

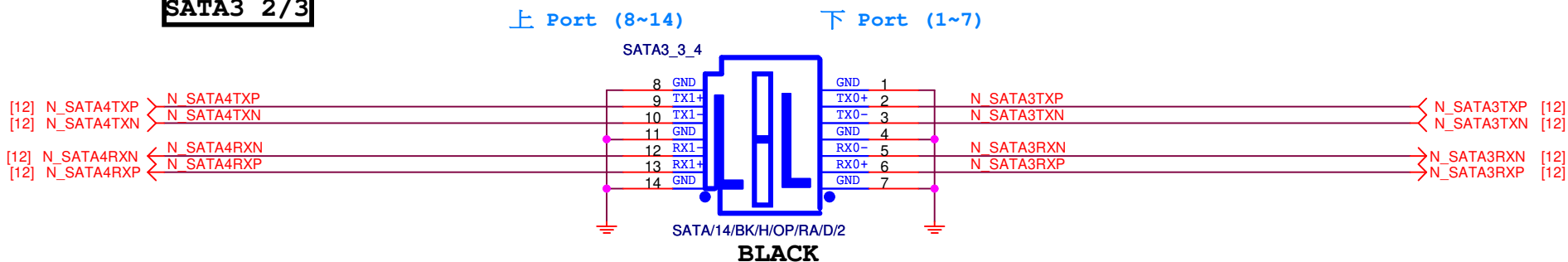
1 SATA3 from Z590 (90度V-A)



Footprint : H2X7-SATA2-D10

SATA3 2/3

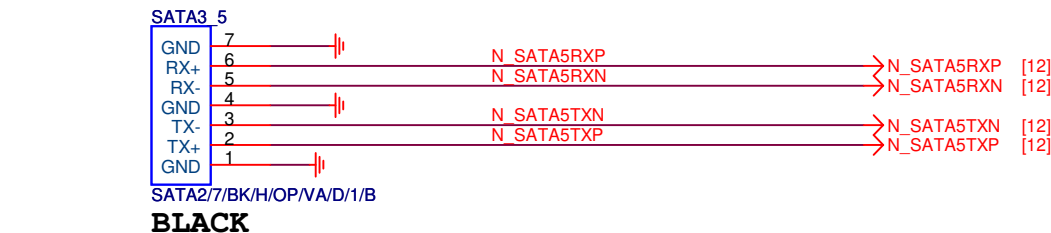
IO21/IO22 To SATA3 port3/4



Footprint : H2X7-SATA2-D10

SATA3 4/5

IO23 To SATA3 port5



Footprint : H1X7-SATA2-HS-MA5K

Gigabyte Technology

Title		
SATA		
Size	Document Number	Rev
Custom	Z590 UD AC	1.01
Date:	Wednesday, December 30, 2020	Sheet 24 of 69

Rev 0.1

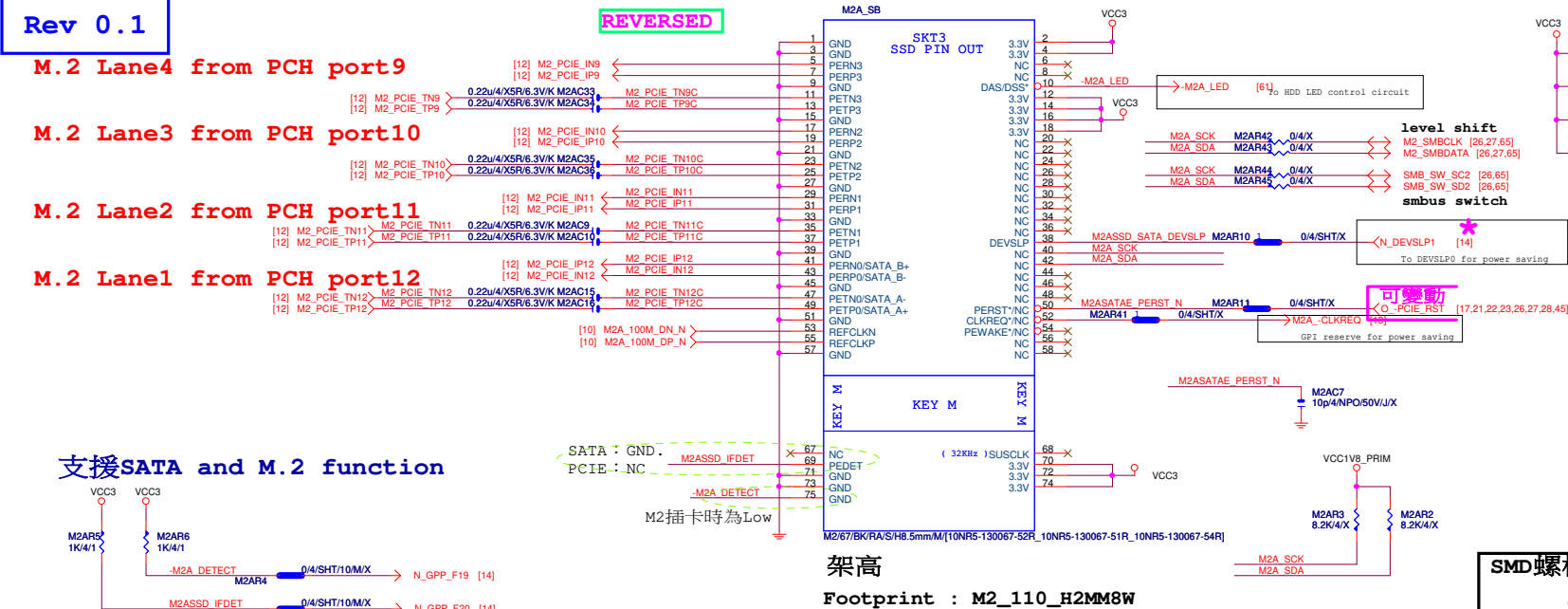
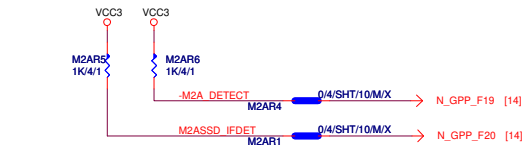
M.2 Lane4 from PCH port9

M.2 Lane3 from PCH port1

M.2 Lane2 from PCH port1

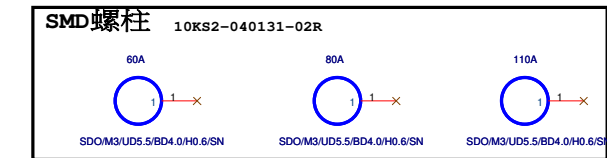
M.2 Lane1 from PCH port1

支援SATA and M.2 function



放在包材裡

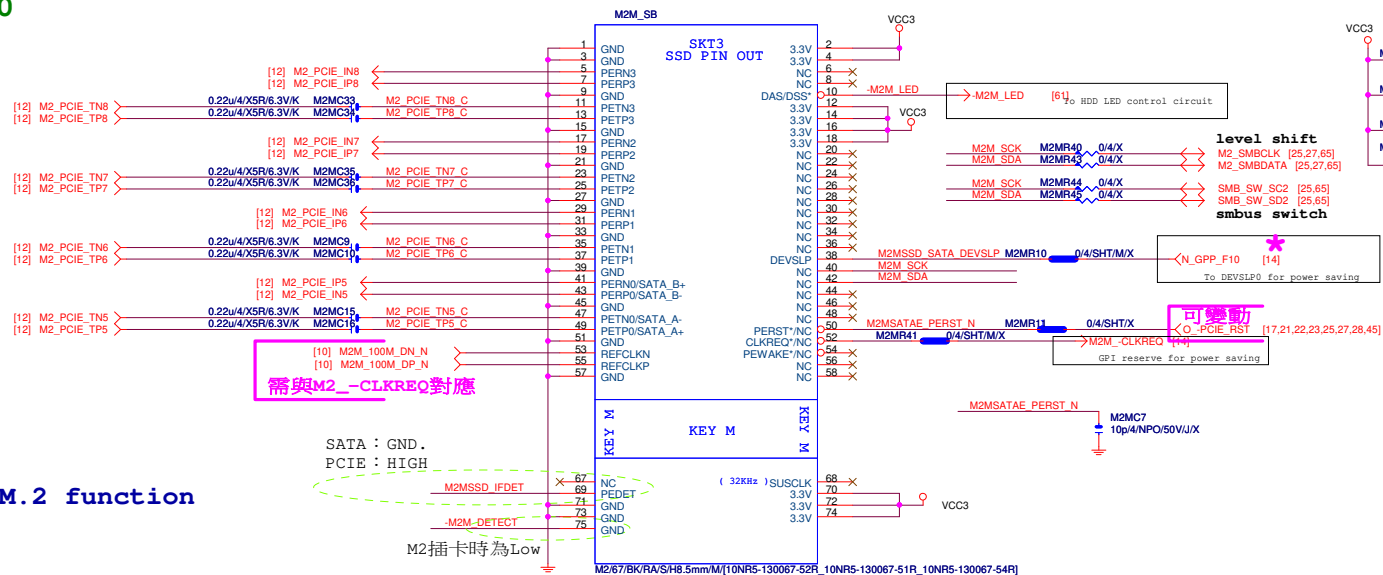
The diagram illustrates two packaging configurations for the CR12KSF-F10303-81R component. The left package, labeled 'DIP 螺柱' (DIP Pin), contains two pins. The right package, labeled 'DIP 螺絲' (DIP Screw), contains one screw. Both packages are marked with '80A' and 'CR{12KS2-110202-31R}X'.



Footprint : HOLE_C236D165-A
10KS2-040131-02R:SDO/M3/UD5.5/BD4.0/H0.6/SN

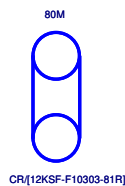
Flex IO priority	N_GPP_F20	IO14 PCIe#9	IO15 PCIe#10	IO16 PCIe#11	IO17 PCIe#12
M2A SATA	L	PCIE	PCIE	SATA 0	SATA 1
M2A PCIe (PCIe Reverse)	H	PCIE	PCIE	PCIE	PCIE

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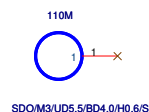
Flex IO priority	N_GPP_F5	IO22 PCIe#17	IO23 PCIe#18	IO24 PCIe#19	IO25 PCIe#20
M2M SATA	L	SATA 4	SATA 5	PCIE	PCIE
M2M PCIE	H	PCIE	PCIE	PCIE	PCIE

DIP螺柱



SMD螺柱

10KS2-040131-02R



Gigabyte Technology

Title	M.2 X4		
Size	Custom	Document Number	Rev 1.01
Date:	Wednesday, December 30, 2020	Sheet 26 of 69	

Rev 0.1

M.2 Lane4 from CPU port4

M.2 Lane3 from CPU port3

M.2 Lane2 from CPU port2

M.2 Lane1 from CPU port1

支援SATA and M.2 function

需與M2_-CLKREQ對應

架高金屬加強
Footprint : M2_110_H2MM8W

DIP螺柱

SMD螺柱

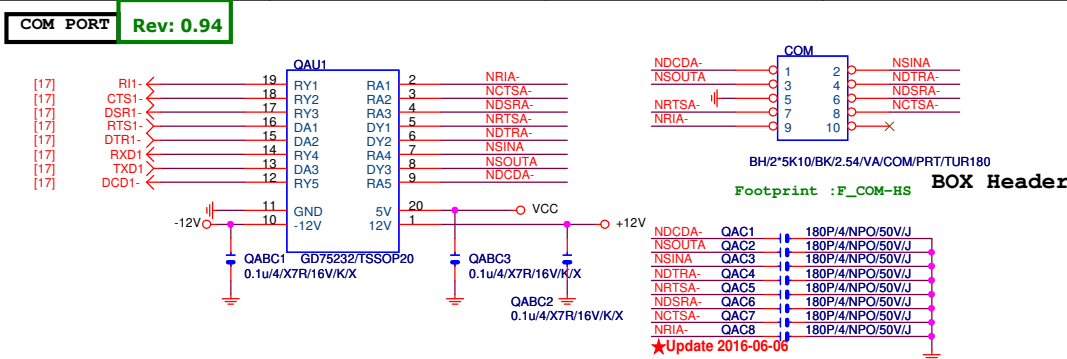
Footprint : HOLE_C236D165-A

SMD螺柱

HS_DIP螺絲

Gigabyte Technology

Title			M.2 X4 (P)
Size	Document Number	Rev	
Custom	Z590 UD AC	1.01	
Date:	Wednesday, December 30, 2020	Sheet	27 of 69

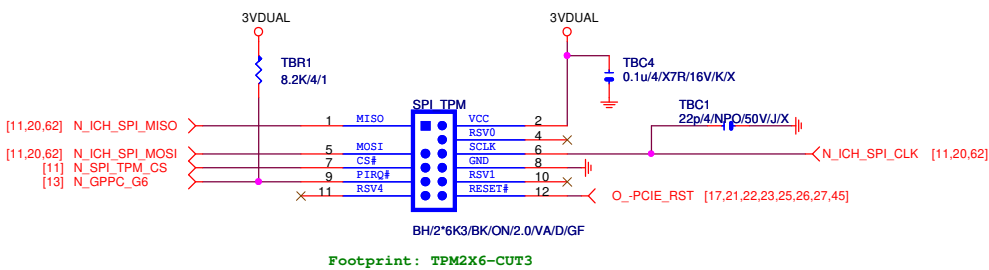


LPT PORT

RTD3 GPIO refer by Intel RVP

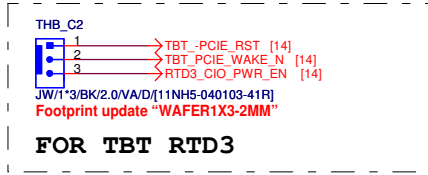
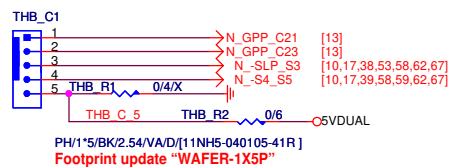
GPIO	CFL-S	CML-U	CML-H	CML-S
TBT_PERST_N	GPP_F_2	GPPC_C15_SLOT1_RST_N	GPP_F4_SATAPCIE7	GPP_F2
TBT_Wake_N	GPP_H_15	GPPC_D11_SLOT1_WAKE_N	GPPK_18	GPP_H15
RTD3_PWN_EN	GPP_I_5	GPPC_D15	GPP_H_16_SML4_CLK	GPP_K23

TPM CONNECT



Thunderbolt

★Update 2015-12-29

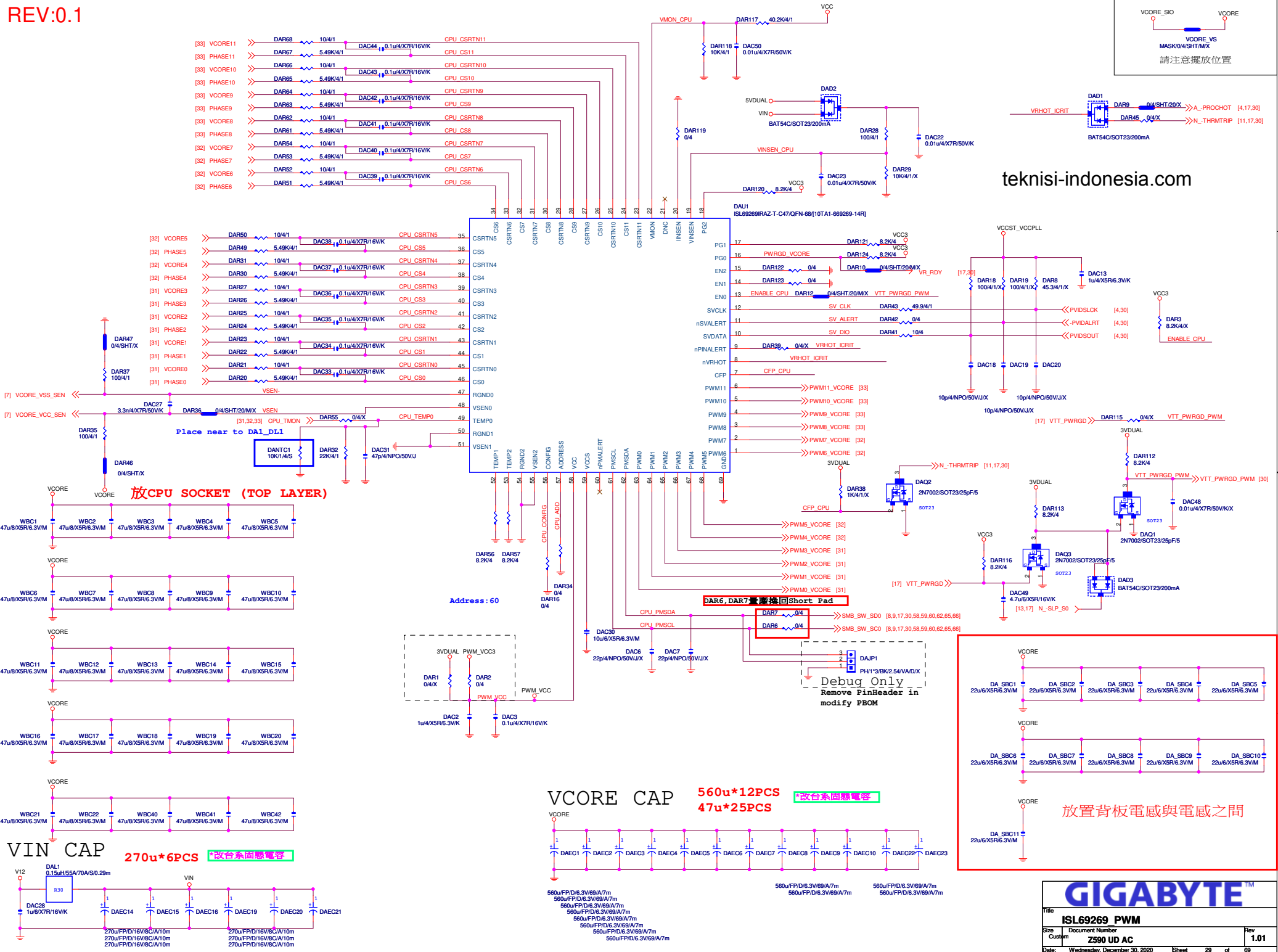


FOR TBT RTD3

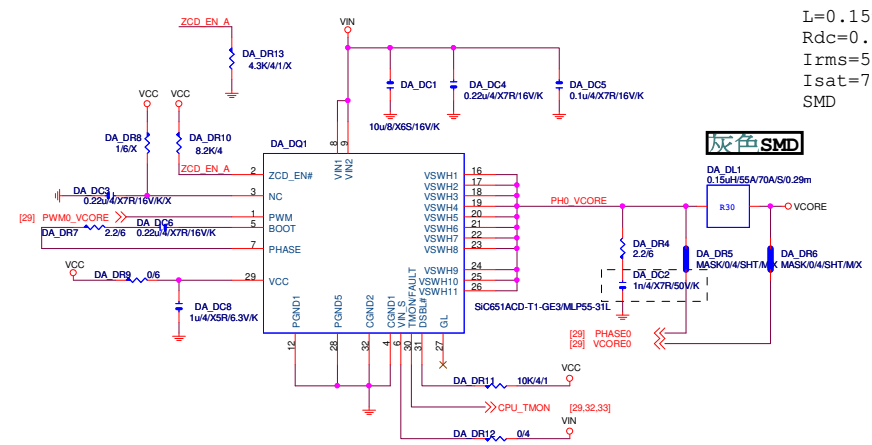
Z490系列使用

TBT_PCIE_RST : CFL connector to GPP_F_2
TBT_PCIE_WAKE_N : CFL connector to GPP_H_15
RTD3_CIO_PWR_EN : CFL connector to GPP_K_3

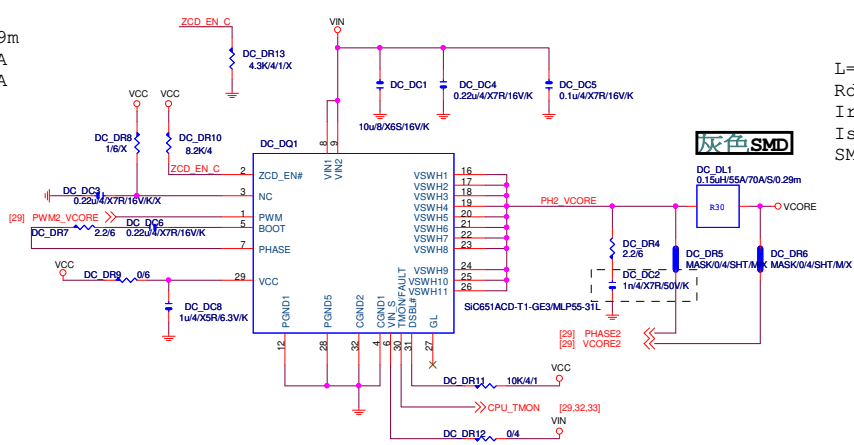
REV:0.1



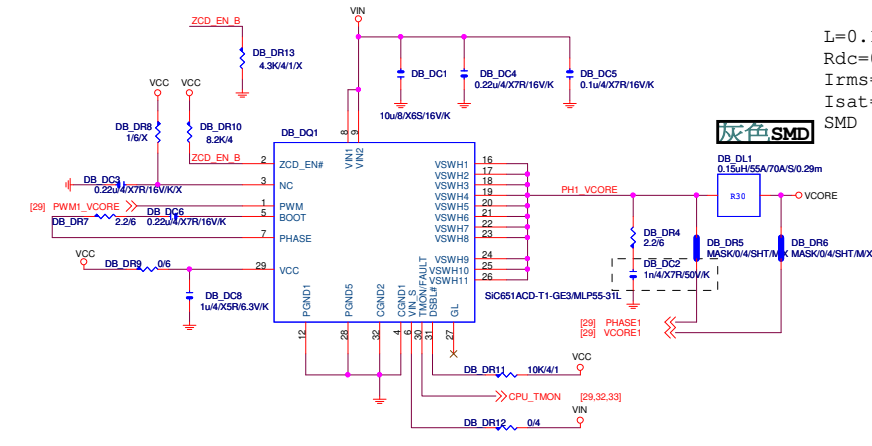
DRMOS使用NCP302155時PIN2 and PIN3要上件 (Ex:DA_DR13.DA_DR8.DA_DC3)



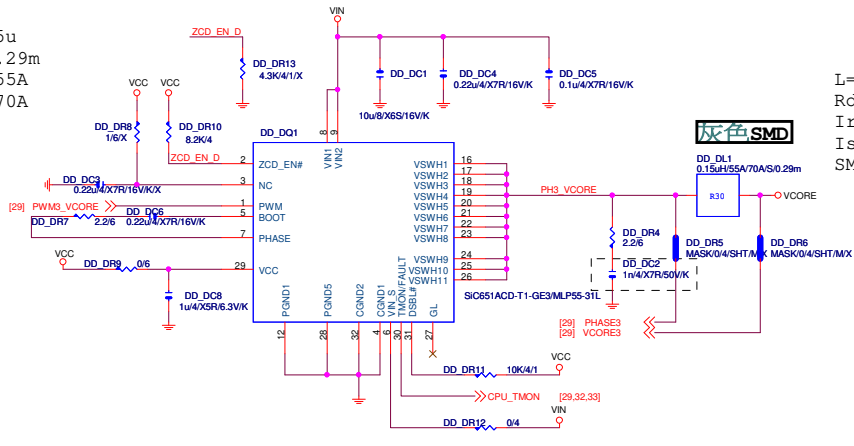
L=0.15u
Rdc=0.29m
Irms=55A
Isat=70A
SMD



L=0.15u
Rdc=0.29m
Irms=55A
Isat=70A
SMD

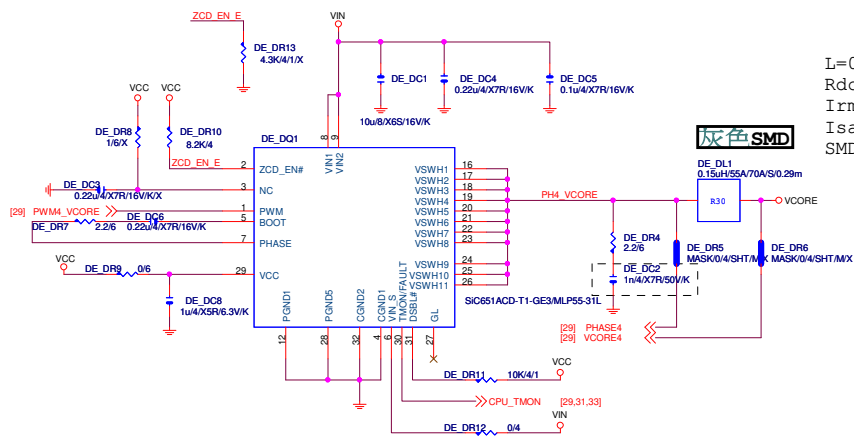


L=0.15u
Rdc=0.29m
Irms=55A
Isat=70A
SMD

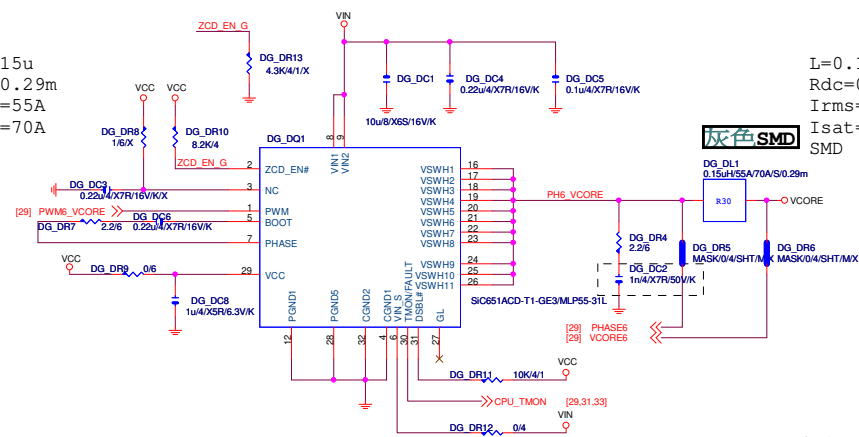


L=0.15u
Rdc=0.29m
Irms=55A
Isat=70A
SMD

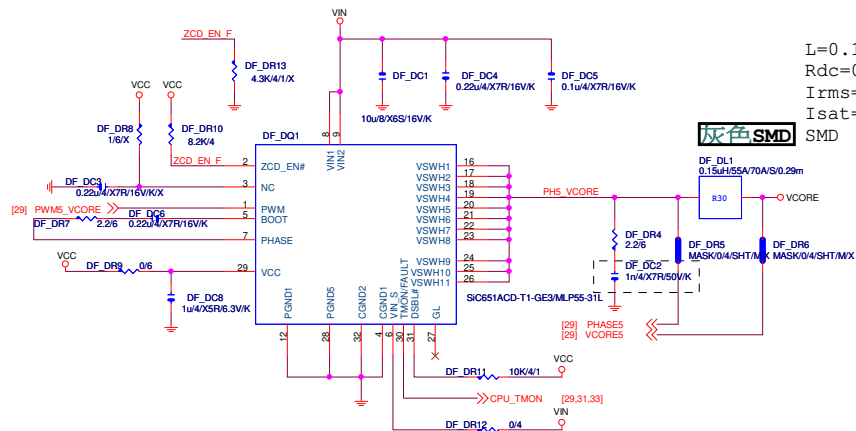
DRMOS使用NCP302155時PIN2 and PIN3要上件(Ex:DA_DR13.DA_DR8.DA_DC3)



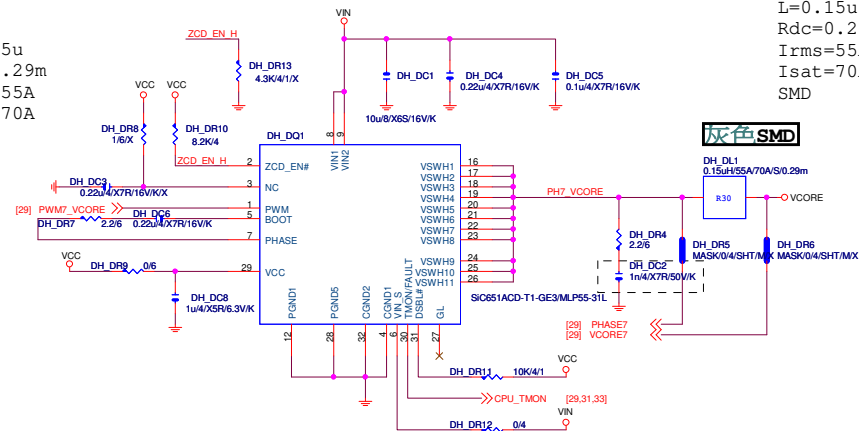
$L=0.15\mu$
 $R_{dc}=0.29m$
 $I_{rms}=55A$
 $I_{sat}=70A$



$L=0.15\mu$
 $R_{dc}=0.29m$
 $I_{rms}=55A$
 $I_{sat}=70A$



$L=0.15\mu$
 $R_{dc}=0.29m$
 $I_{rms}=55A$
 $I_{sat}=70A$



$L=0.15\mu$
 $R_{dc}=0.29m$
 $I_{rms}=55A$
 $I_{sat}=70A$

GIGABYTE™

File			VCORE DRMOS-2
Size	Document Number	Rev	1.01
Custom	Z590 UD AC		
Date:	Wednesday, December 30, 2020	Sheet	32 of 69



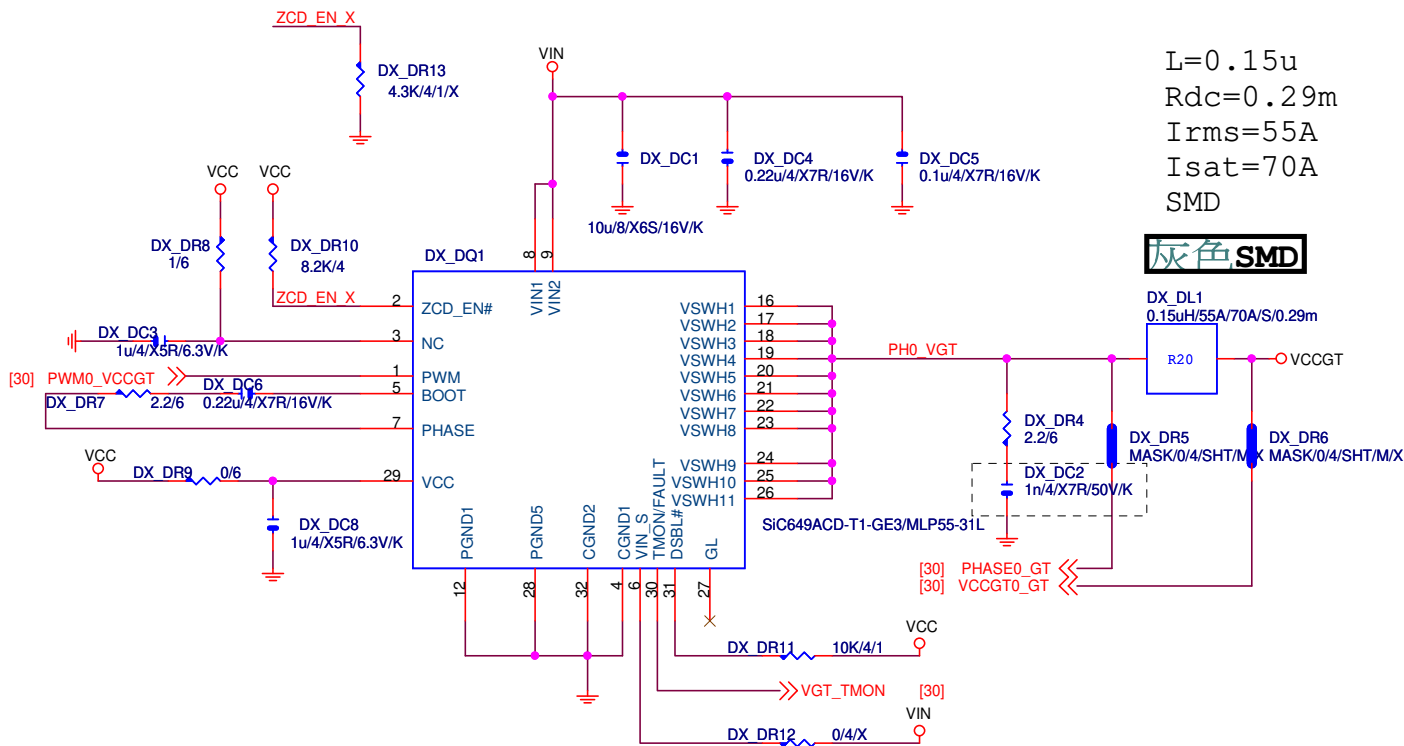
放CPU SOCKET (Bottom LAYER)

GIGABYTE™

Title			
VCORE_DRMOS-3			
Size	Document Number	Rev	
Custom	7590 UD AC	1.01	
Date:	Wednesday, December 30, 2020	Sheet	33 of 69

REV:0.1

DRMOS使用NCP302155時PIN2 and PIN3要上件 (Ex:DA_DR13.DA_DR8.DA_DC3)



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GIGABYTE™

Title

VCCGT_DRMOS

Size

Document Number

Custom

Z590 UD AC

Rev

1.01

Date:

Wednesday, December 30, 2020

Sheet

34

of

69

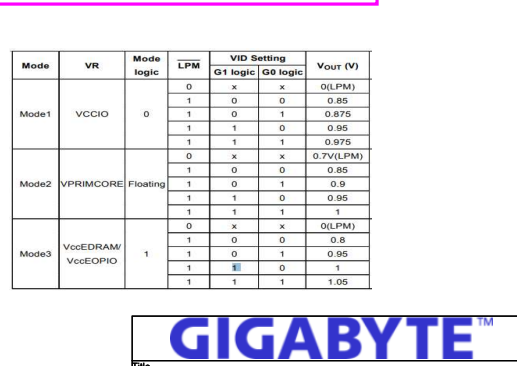
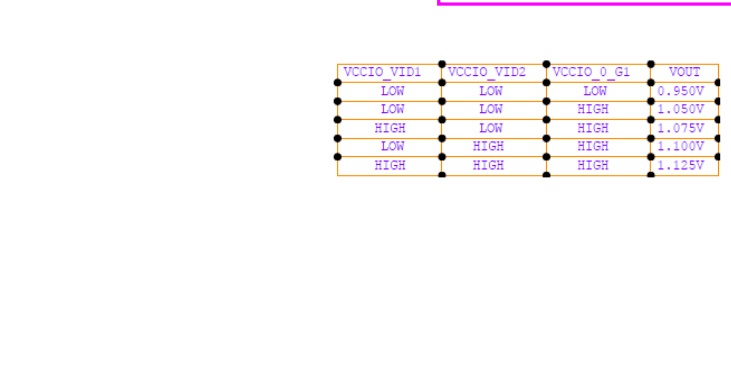
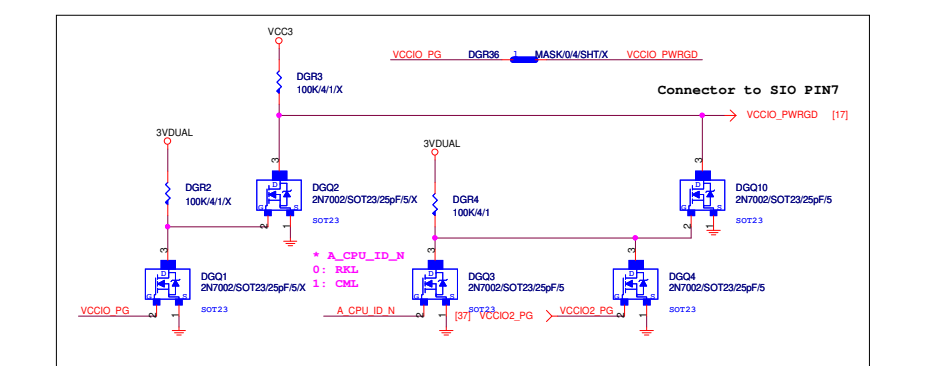
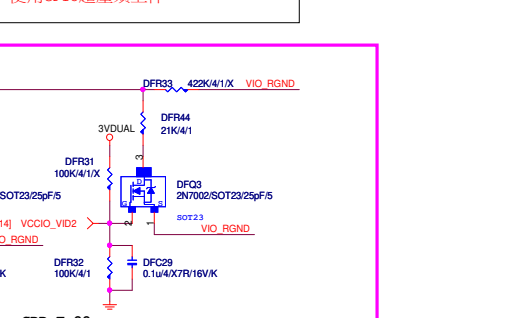
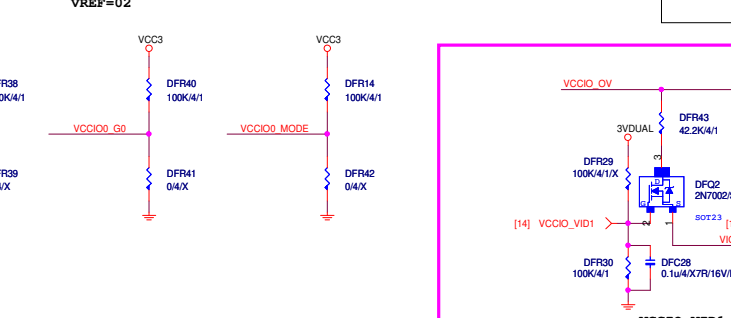
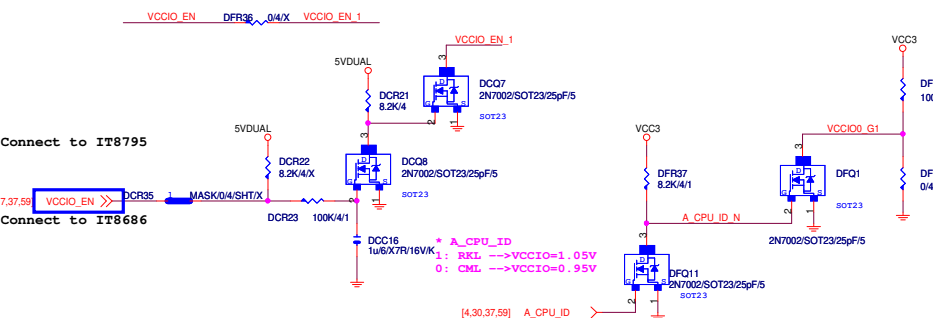
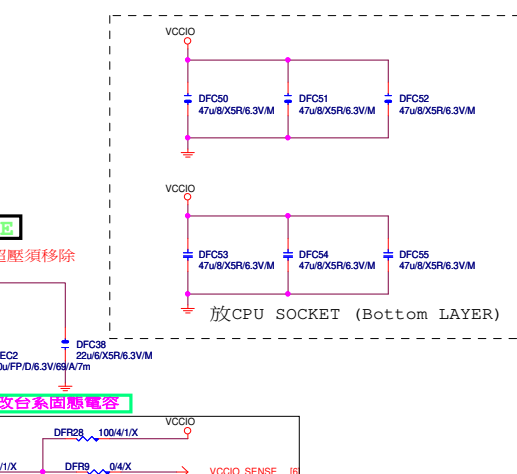
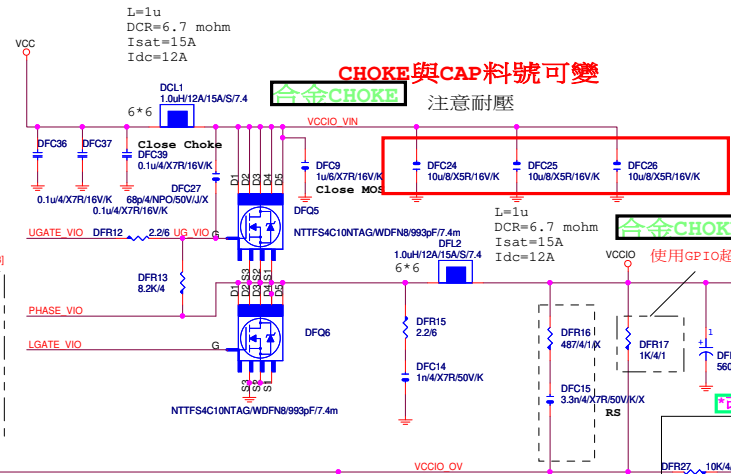
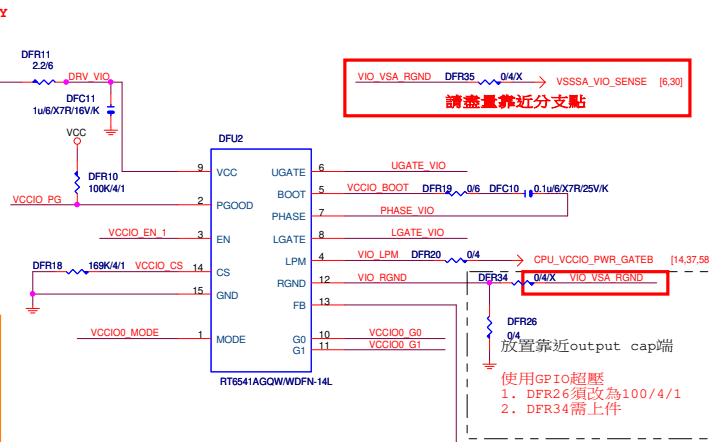
VCCIO

REV:0.2

RKL MODIFY

VIO_VSA_RGND DFR35 04/X VSSA_VIO_SENSE [6,30]
請盡量靠近分支點

RKL MODIFY
VCC1V8_P8IM
DFR24 8.2K/4/X
VIO_LPM

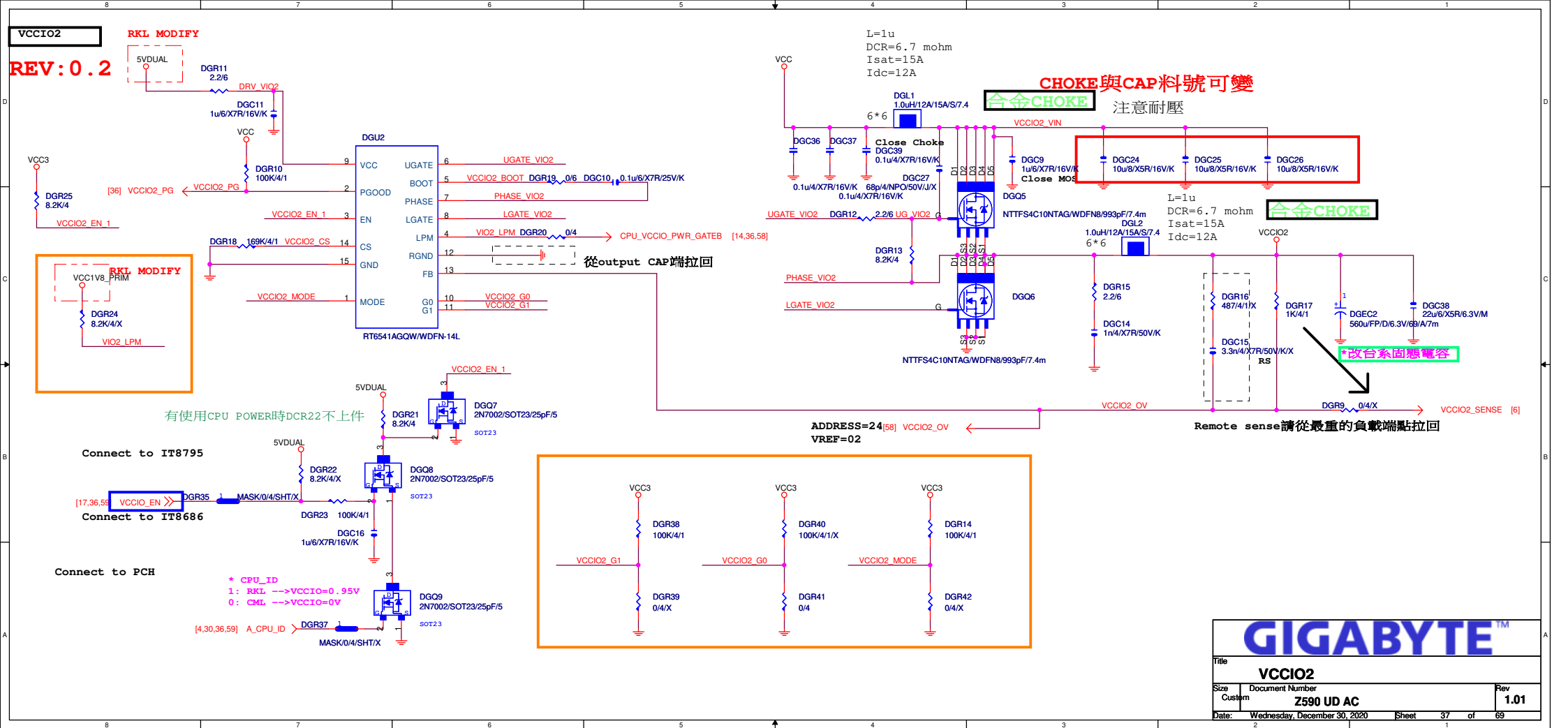


VCCIO_VID1	VCCIO_VID2	VCCIO_0_G1	VOUT
LOW	LOW	LOW	0.950V
LOW	LOW	HIGH	1.050V
HIGH	LOW	HIGH	1.075V
LOW	HIGH	HIGH	1.100V
HIGH	HIGH	HIGH	1.125V

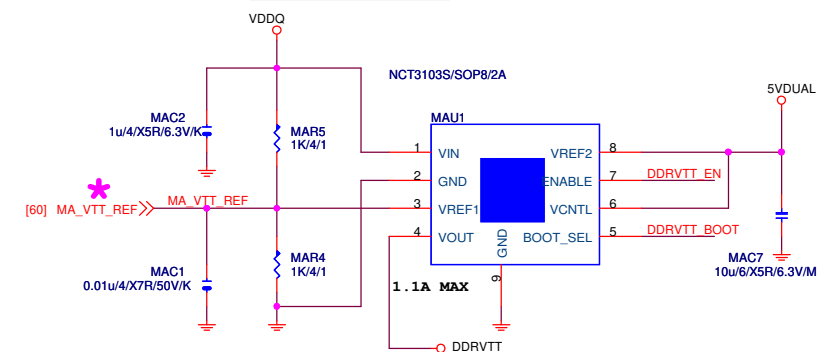
Mode	VR	Mode logic	LPM	VID Setting		Vout (V)
				G1 logic	G0 logic	
Mode1	VCCIO	0	0	x	x	0(LPM)
			1	0	0	0.85
			1	0	1	0.875
			1	1	0	0.95
			1	1	1	0.975
Mode2	VPRIMCORE	Floating	0	x	x	0.7V(LPM)
			1	0	0	0.85
			1	0	1	0.9
			1	1	0	0.95
			1	1	1	1
Mode3	VccEDRAM/ VccEOPIO	1	0	x	x	0(LPM)
			1	0	0	0.8
			1	0	1	0.95
			1	1	0	1
			1	1	1	1.05

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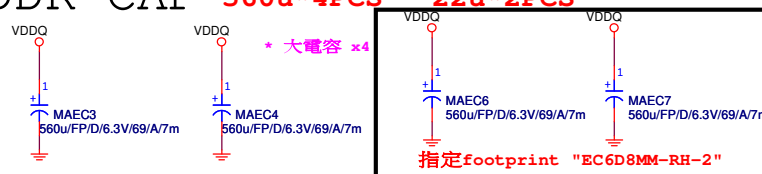
Title	VCCIO		
Size	Document Number	Z590 UD AC	
Custom			Rev 1.01
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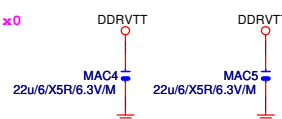
DDR4



DDR	CAP	560u*4PCS	22u*2PCS
-----	-----	-----------	----------



DDRVTT CAP



GIGABYTE™

RT8120 DDR4 POWER

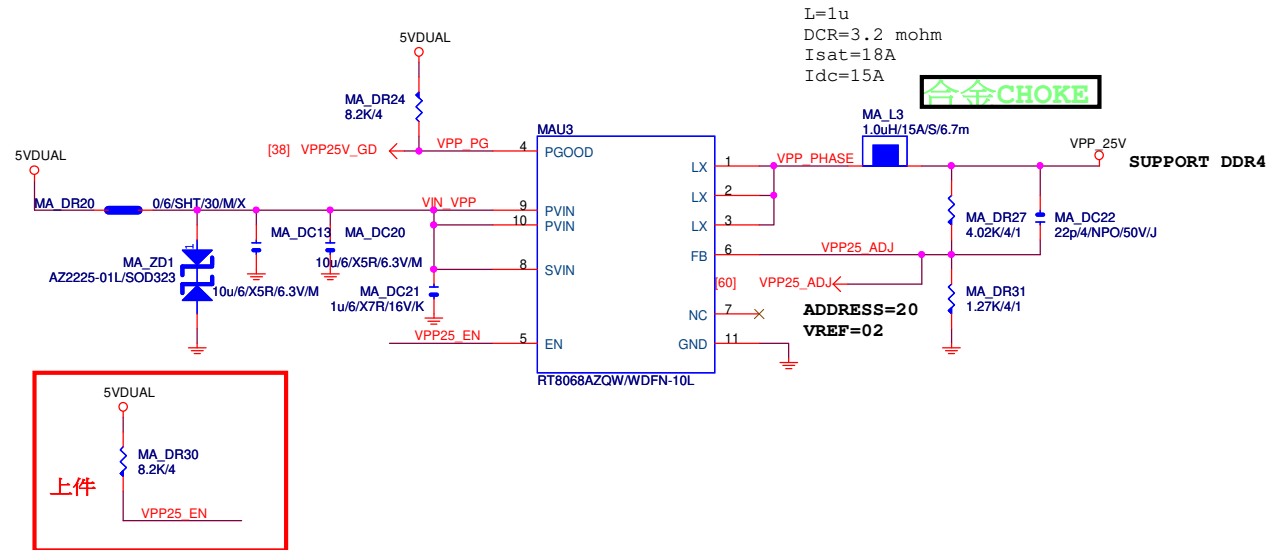
Size Custom	Document Number Z590 UD AC	Rev 1.01
Date:	Wednesday, December 30, 2020	Sheet 38 of 69

Date: Wednesday, December 30, 2020 Sheet 38 of 69

REV:0.1

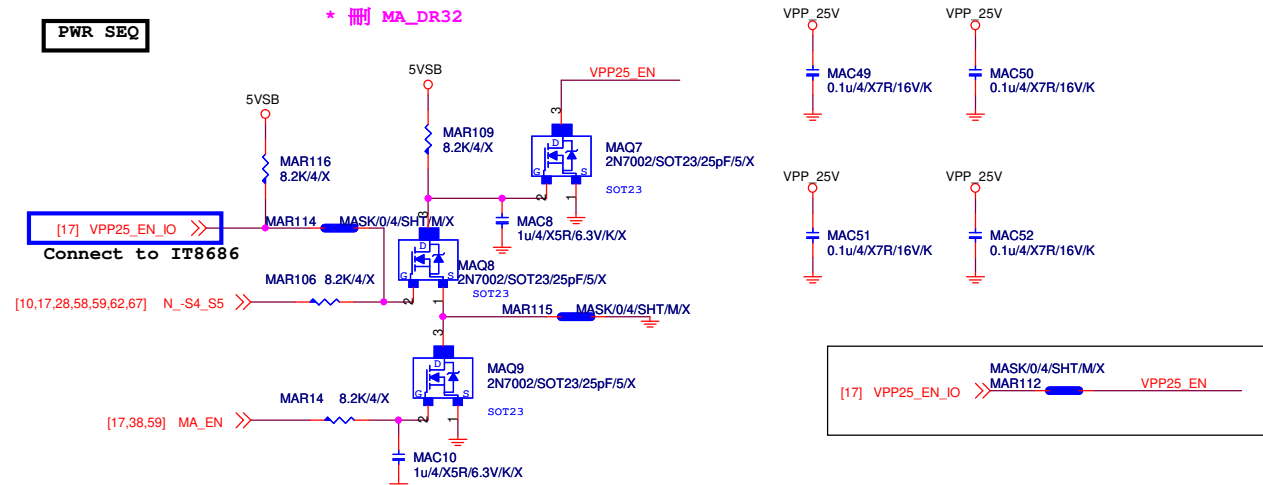
VPP 25V

CHOKE與CAP料號可變

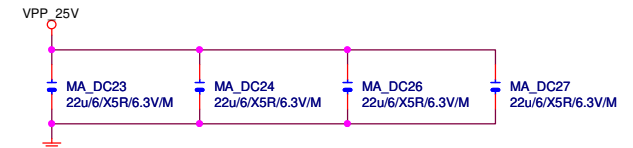


PWR SEQ

* 刪 MA_DR32



VPP CAP 22u*4PCS

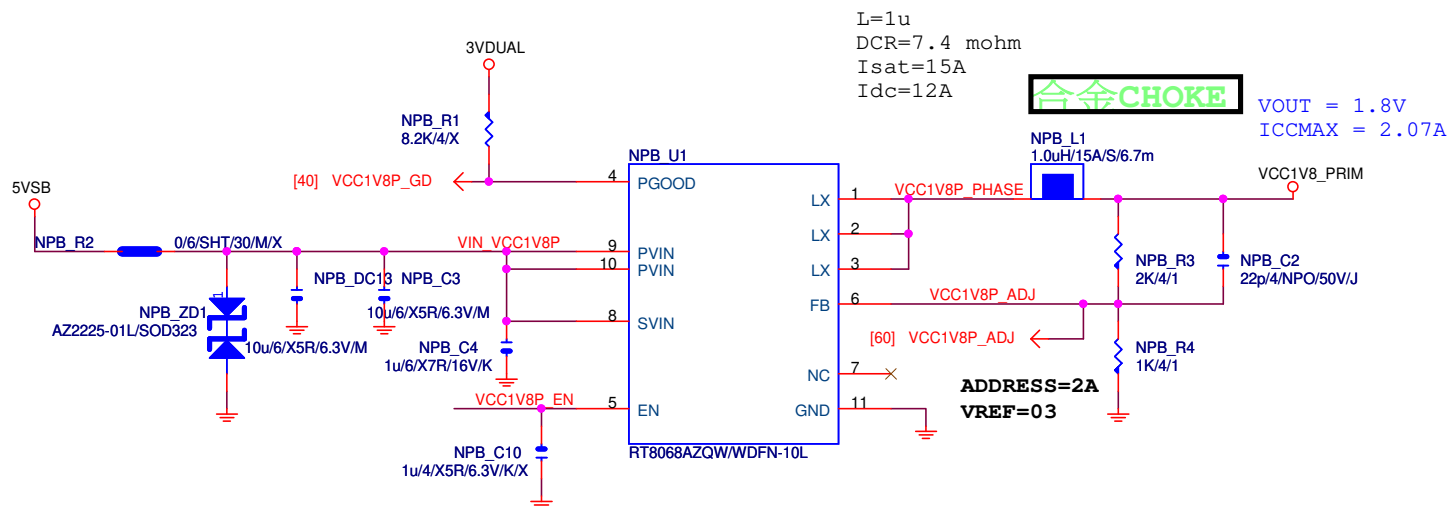


GIGABYTE™

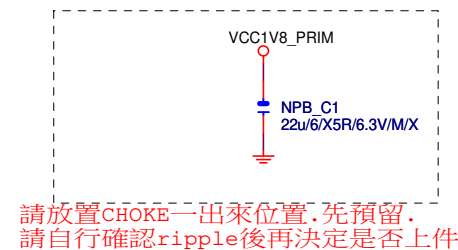
Title			RT8068_VPP25 POWER	
Size	Document Number	Z590 UD AC		Rev
Custom				1.01
Date:	Wednesday, December 30, 2020	Sheet	39 of 69	

REV: 0.1

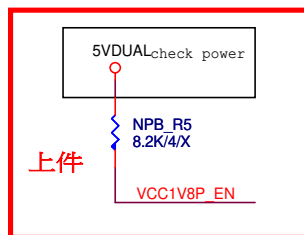
VCC1V8 PRIM



CHOKE與CAP料號可變



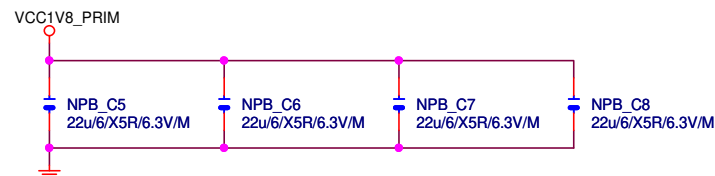
PWR SEQ



connect to PCH pin AD46



VCC1V8_PRIM CAP 22u*4PCS



GIGABYTE™

Title
RT8068_VCC1V8_PRIM

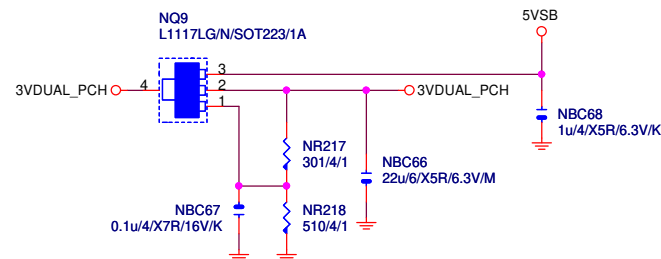
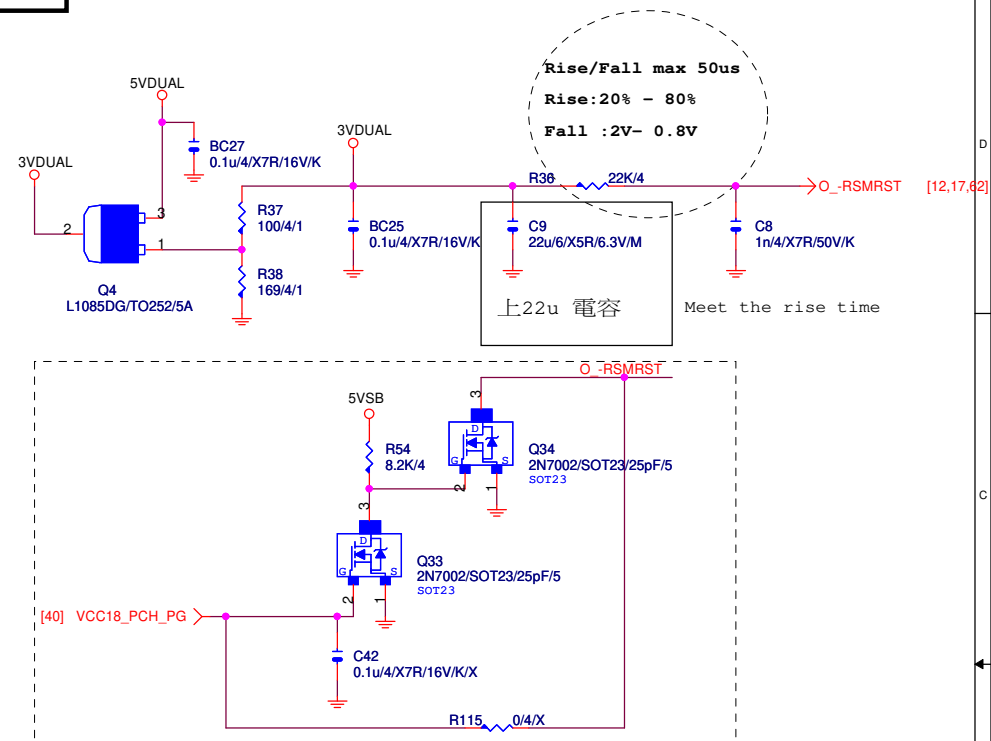
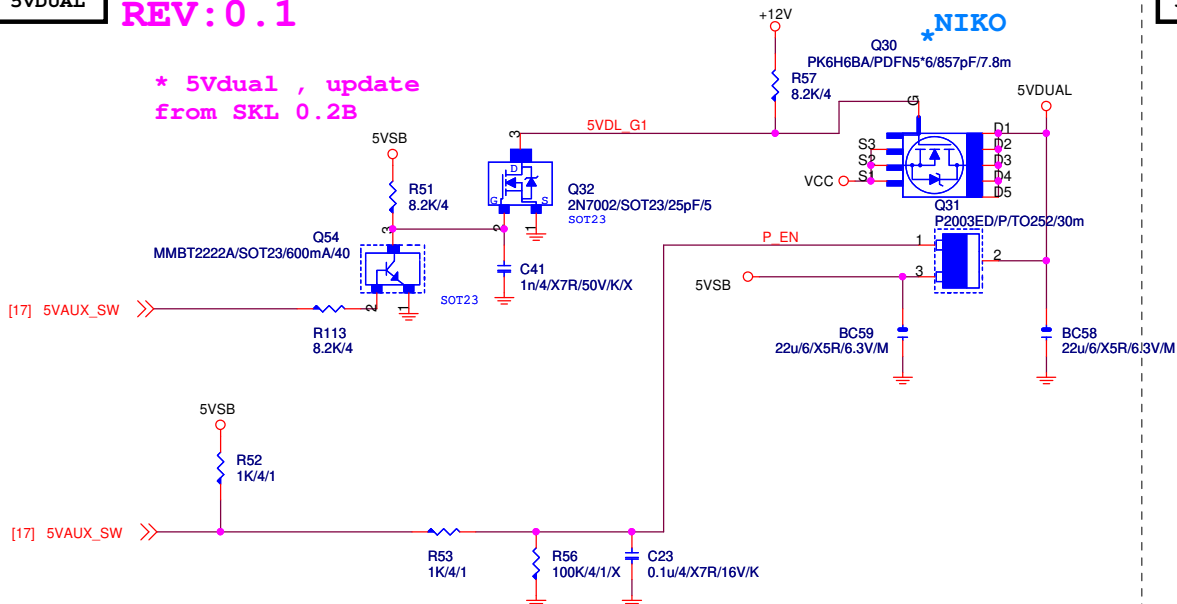
Size Document Number
Custom **Z590 UD AC**

Rev
1.01

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REV: 0.1

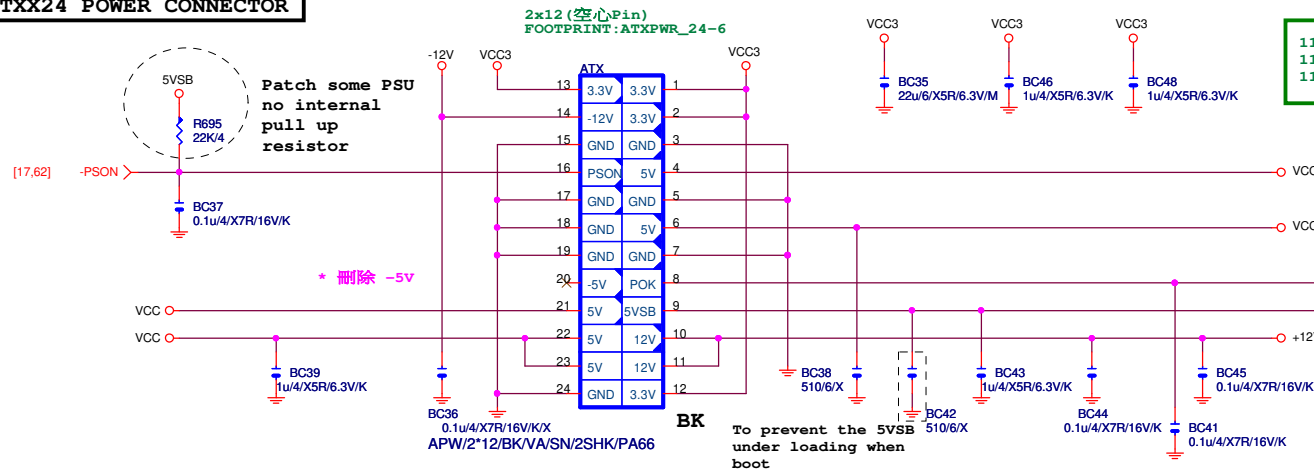
[17] 5VAUX_SW



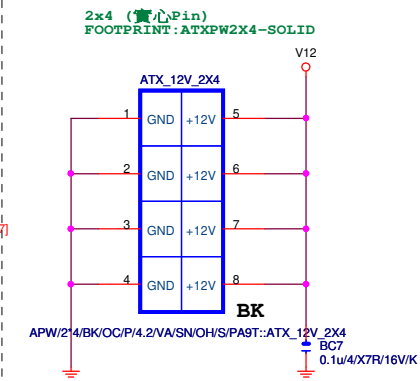
Gigabyte Technology

Title			
DISCRETE POWER			
Size	Document Number		Rev
Custom	Z590 UD AC		1.01
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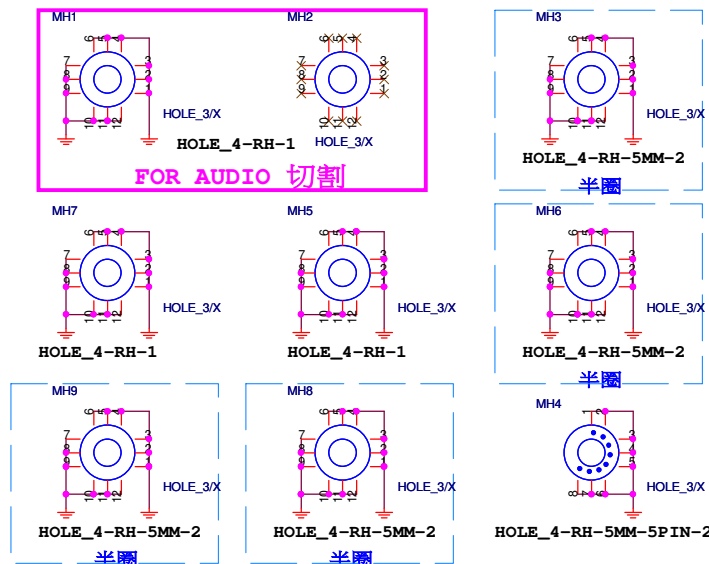
ATXX24 POWER CONNECTOR



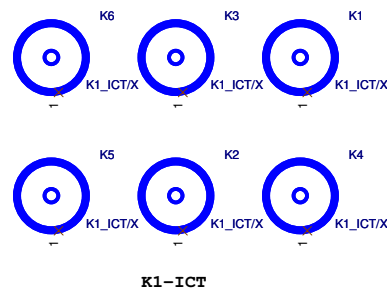
ATXX4 POWER CONNECTOR



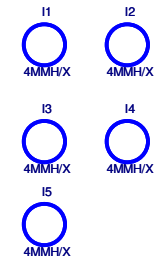
螺絲孔



固定孔/光學點

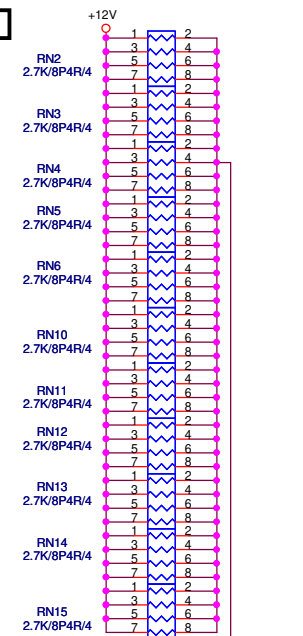
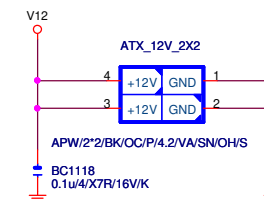


To prevent the 5VSB
under loading when
boot

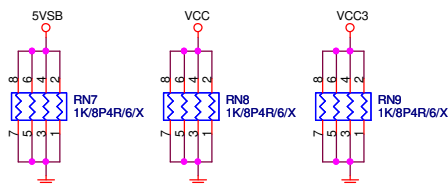


+12V DUMMY LOAD

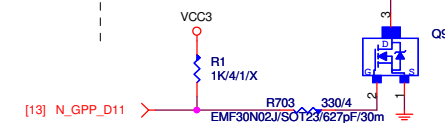
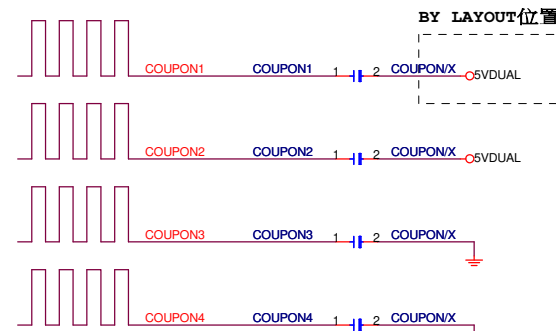
To fix 12V light load
abnromal issue



DUMMY LOAD



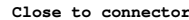
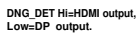
COUPON



Gigabyte Technology

Title	ATX POWER CONNECTOR
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Size	Document Number	Rev
Custom	Z590 UD AC	1.01
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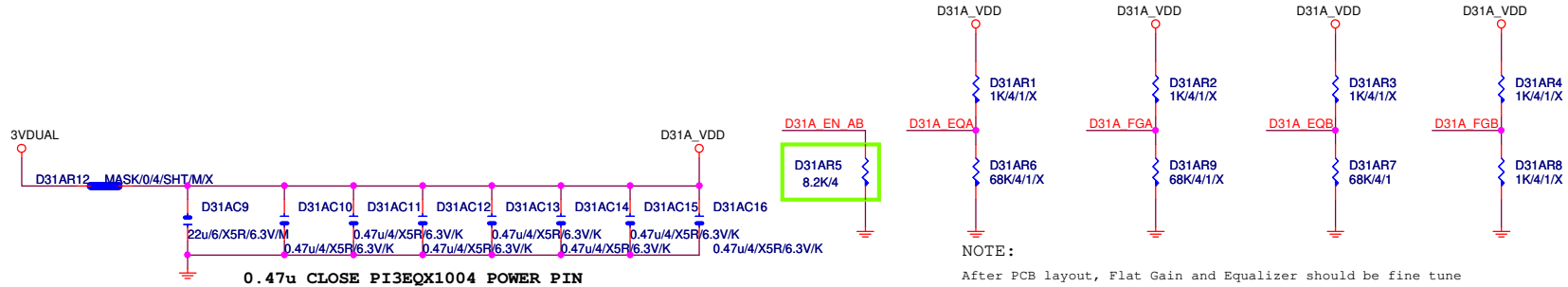


GIGABYTE™			
Title: CNVI_M2_WIFI			
Size	Document Number	Rev	
Custom	Z590 UD AC	1.01	
Date:	Wednesday, December 30, 2020	Sheet	45 of 69

USB3.2 GEN2 PI3EQX1004E Rev0.1

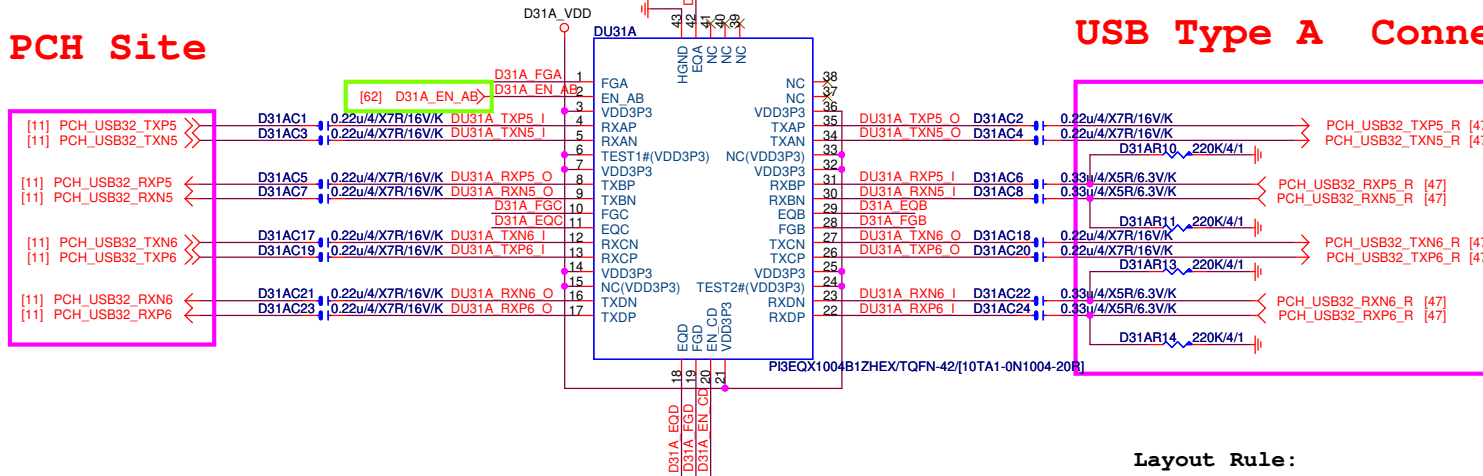
Type-A

GROUP A



PCH Site

USB Type A Connector Site

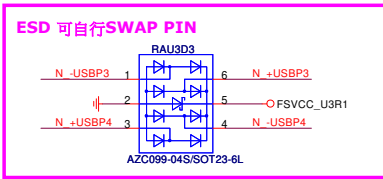
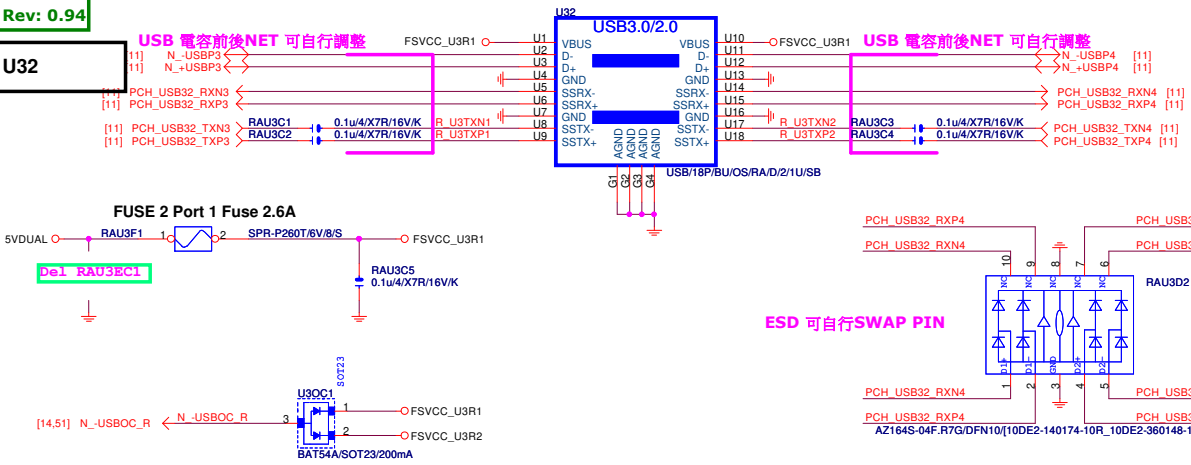


Layout Rule:

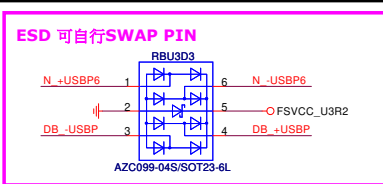
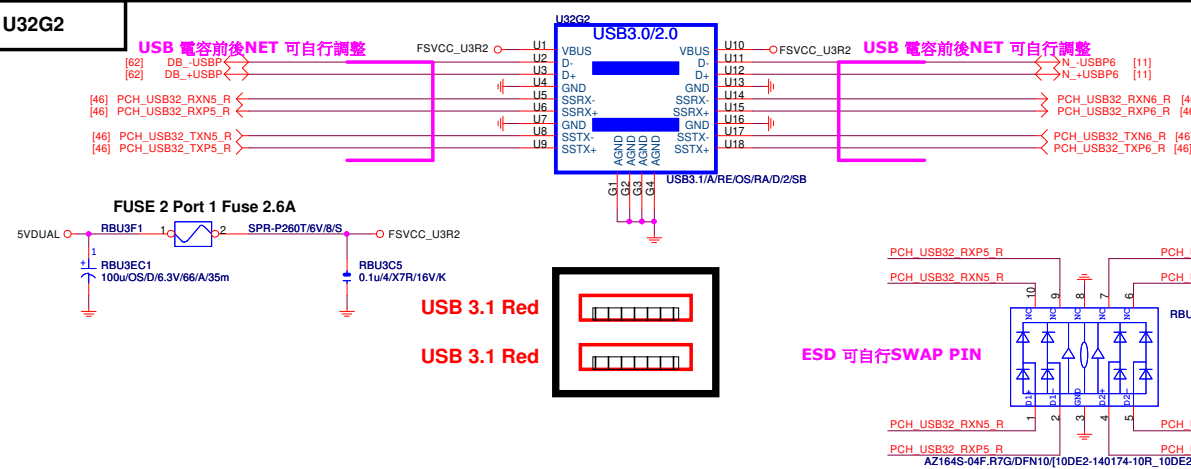
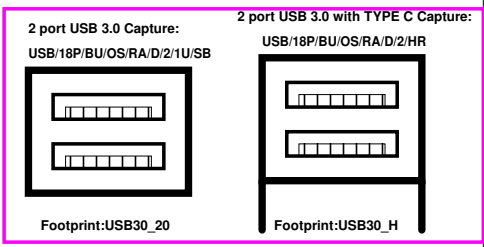
1. Differential Pair can't be swaped
2. Redriver to Connector Length min. 1 inch
3. PCH to Redriver Length min. 6 inch

GIGABYTE™

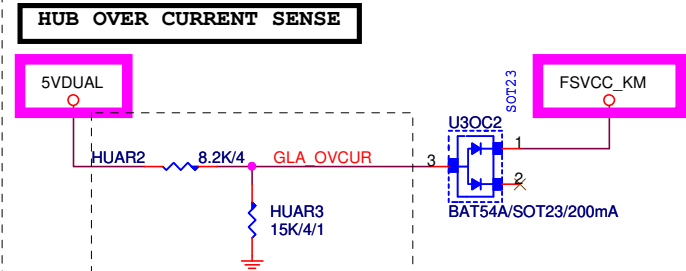
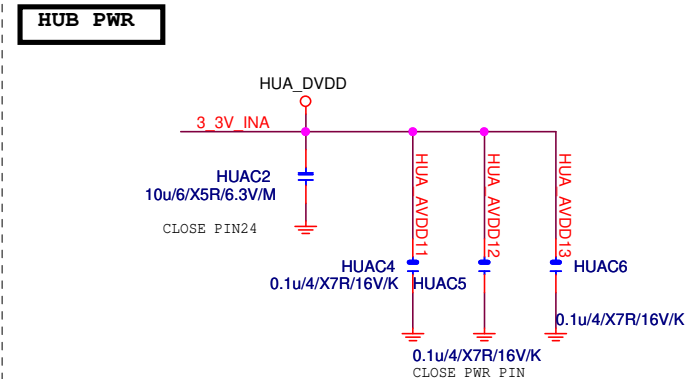
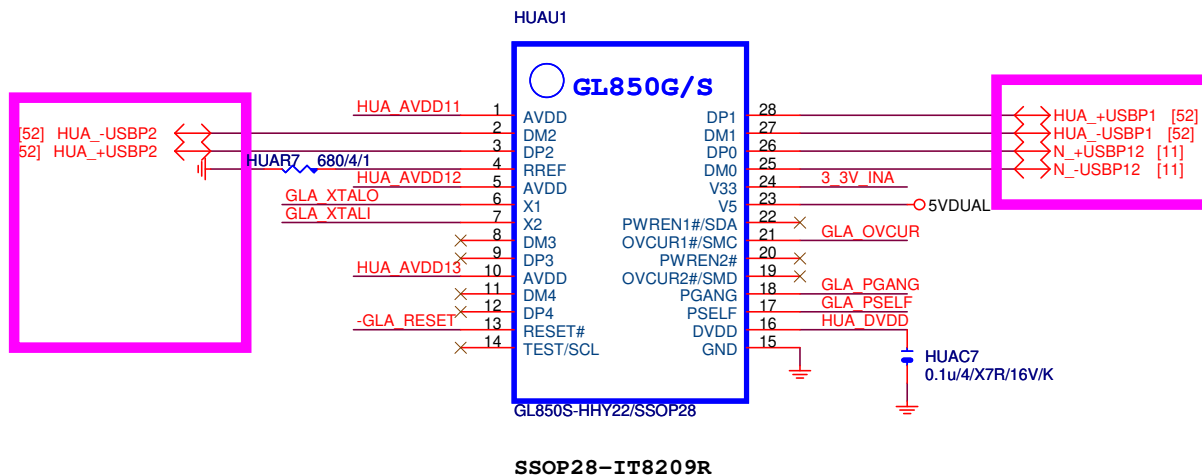
Title		
Redriver_A_Type-A		
Size	Document Number	Rev
B	Z590 UD AC	1.01
Date:	Wednesday, December 30, 2020	Sheet 46 of 69



CONNECTOR 自行調整

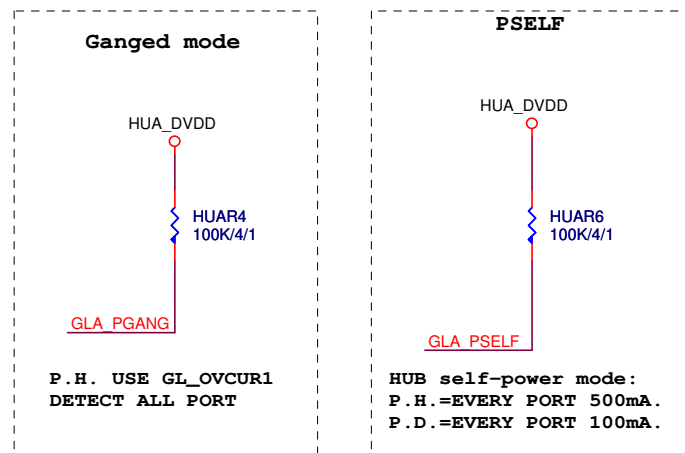


KB_MS_U32

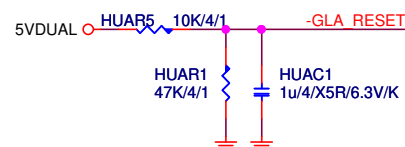


GL850S的over current pin請接到GL850S不要接到PCH, PCH端改為pull-high 3VDUAL.

HUB MODE

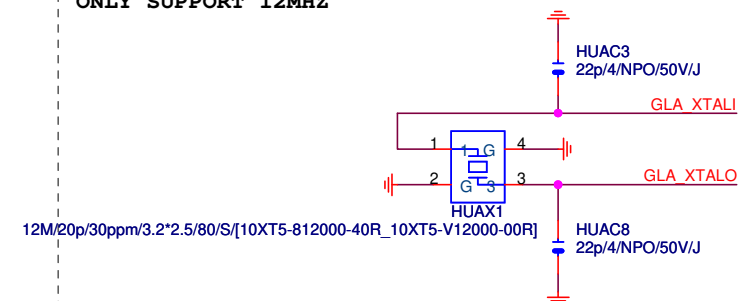


HUB RESET

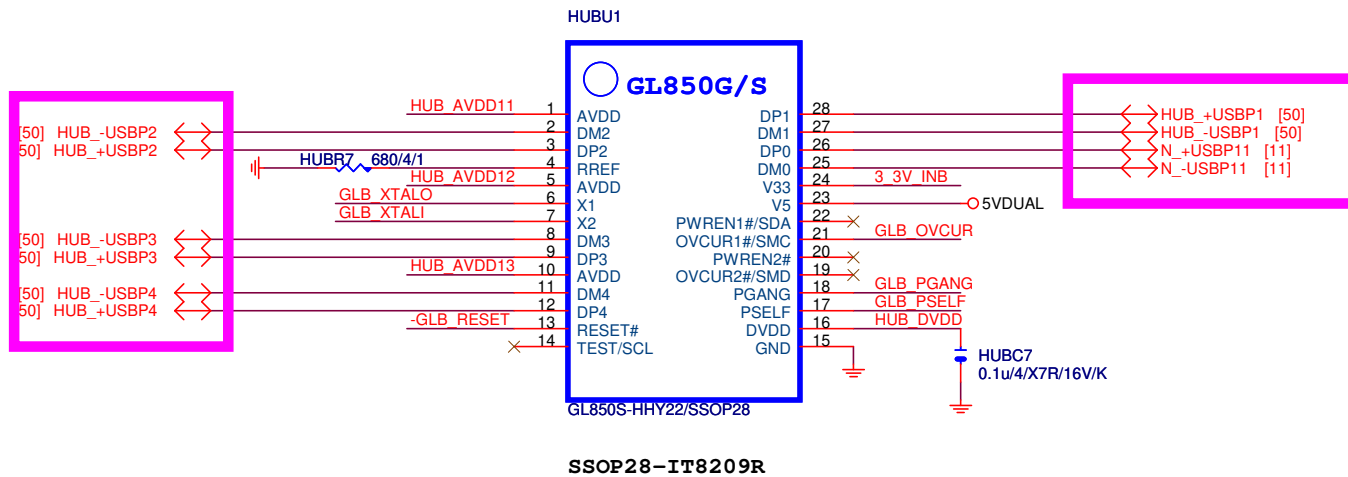


HUB CRYSTAL

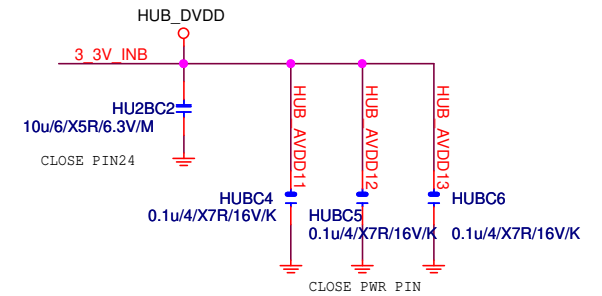
ONLY SUPPORT 12MHZ



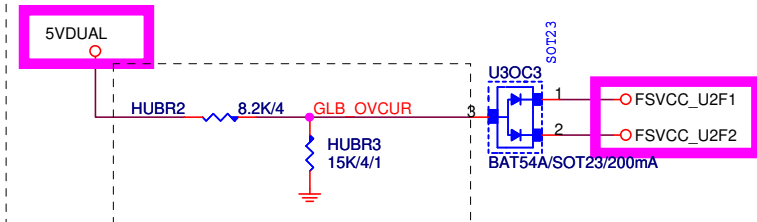
Dual USB2 HUB used Rev 0.1



HUB PWR

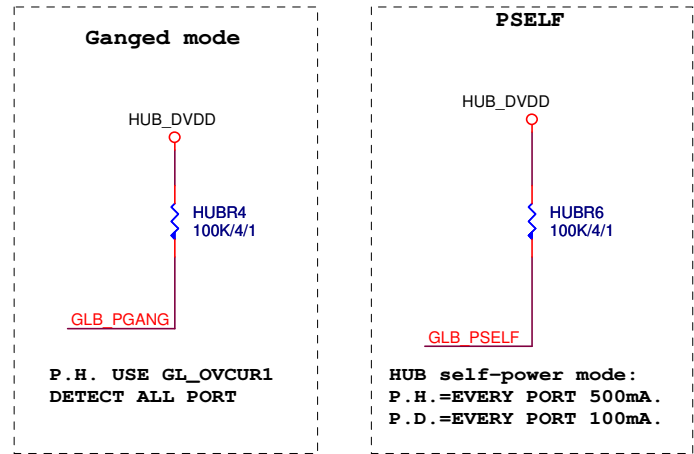


HUB OVER CURRENT SENSE

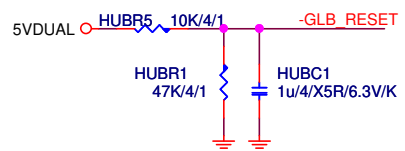


GL850S的over current pin請接到GL850S不要接到PCH, PCH端改為pull-high 3VDUAL.

HUB MODE



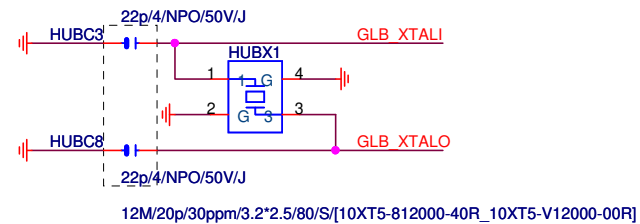
HUB RESET



HUB CRYSTAL

ONLY SUPPORT 12MHZ

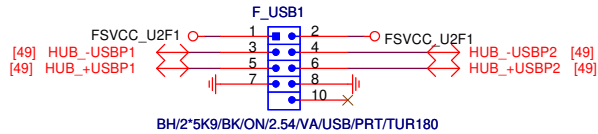
teknisi-indonesia.com



Gigabyte Technology			
Title			
HUB GL850GS_2			
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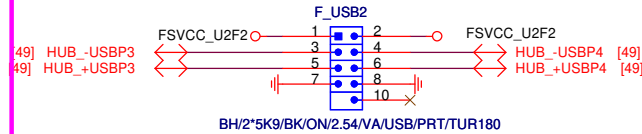
FRONT USB1

NET 可變

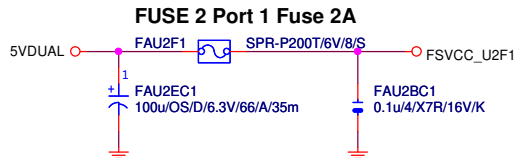


FRONT USB2

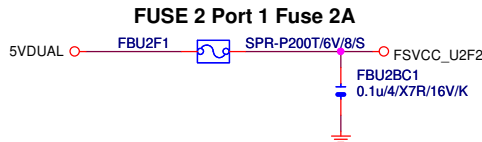
NET 可變



Close to connector
FUSE 2 Port 1 Fuse 2A

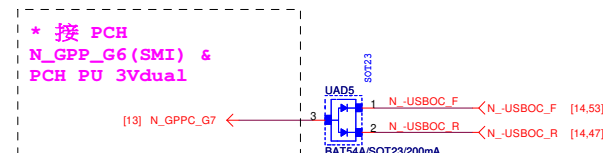
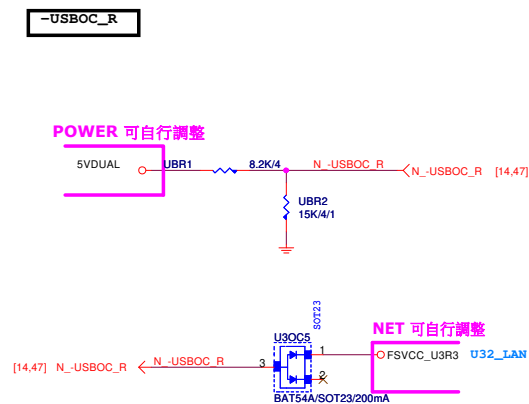
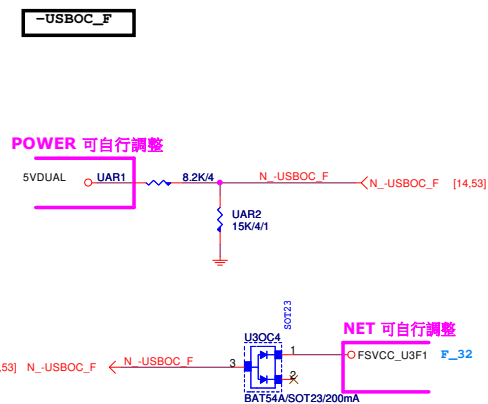
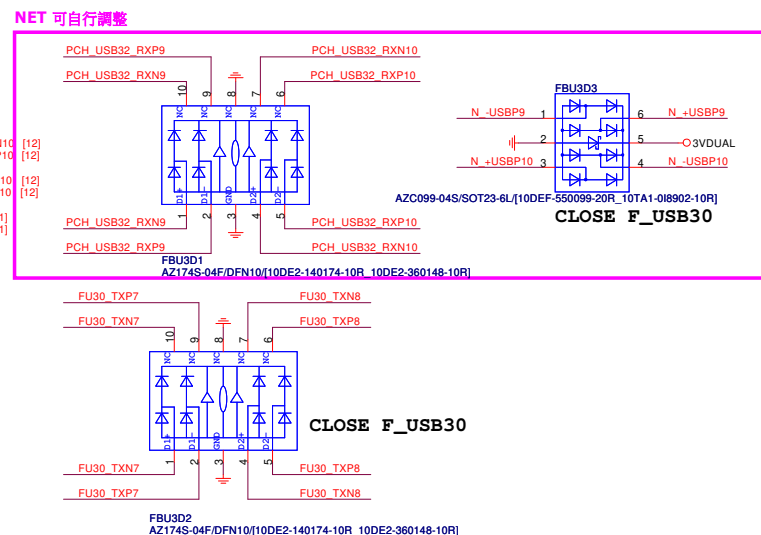
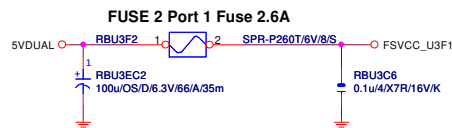
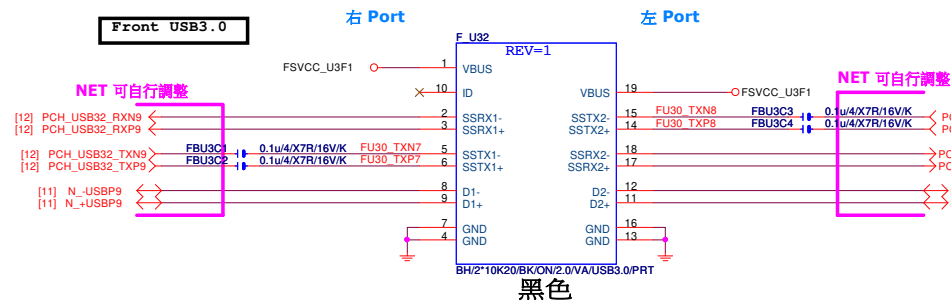


Close to connector
FUSE 2 Port 1 Fuse 2A



Gigabyte Technology

Title		
USB2.0		
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Gigabyte Technology

KB MS USB

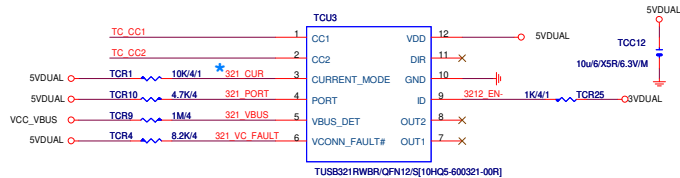
Document Number

Z590 UD AC

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CURRENT MODE

L - Default current / Pull down to GND or NC
M - Medium (1.5A) current / Pull up to VDD 500K
H - High (3.0A) current / Pull up to VDD 10K

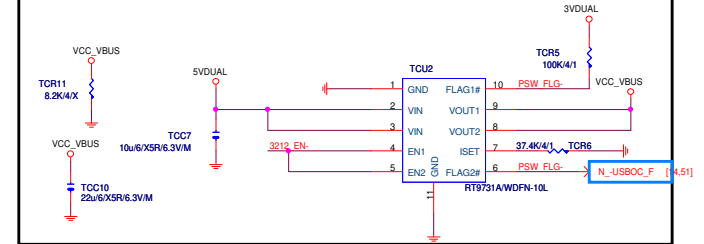
PORT

H - HOST
L - Device
NC - Dual Role

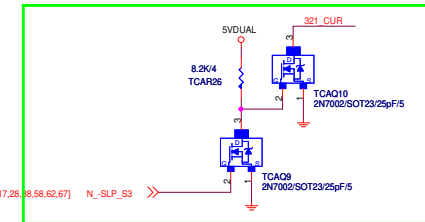
USB POWER

note: 可變更FUSB

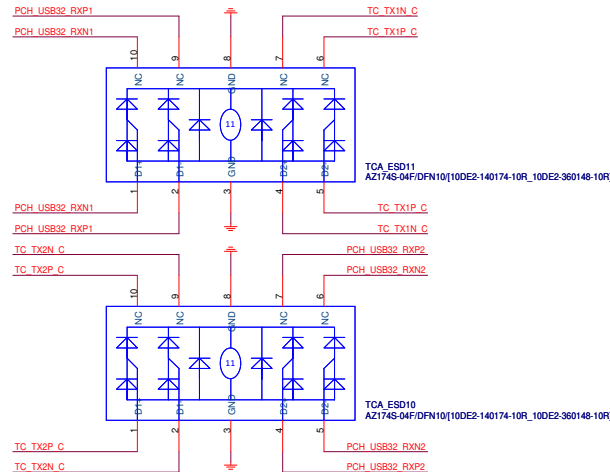
TypeC default 5V/3A



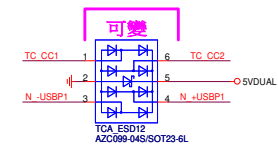
For VBUS current limit at 900mA on S3



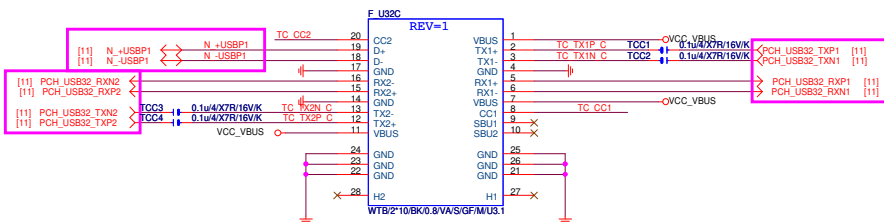
Color markers can be changed by model



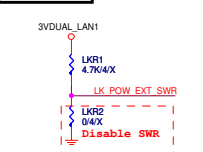
note: 可變更USB NAME



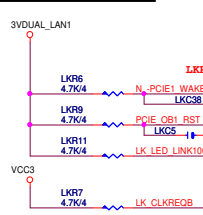
USB2.0 can be used the same source



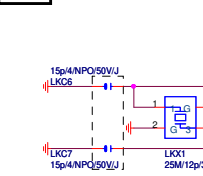
POW_MODE



External Resistor



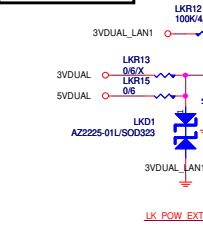
25M SMD Type



SWR



EXTERNAL (0.9V)



External SWR for RTL8125BS SWR disabled

FOR 8125B(S)

FOR 8125BS (SWR)

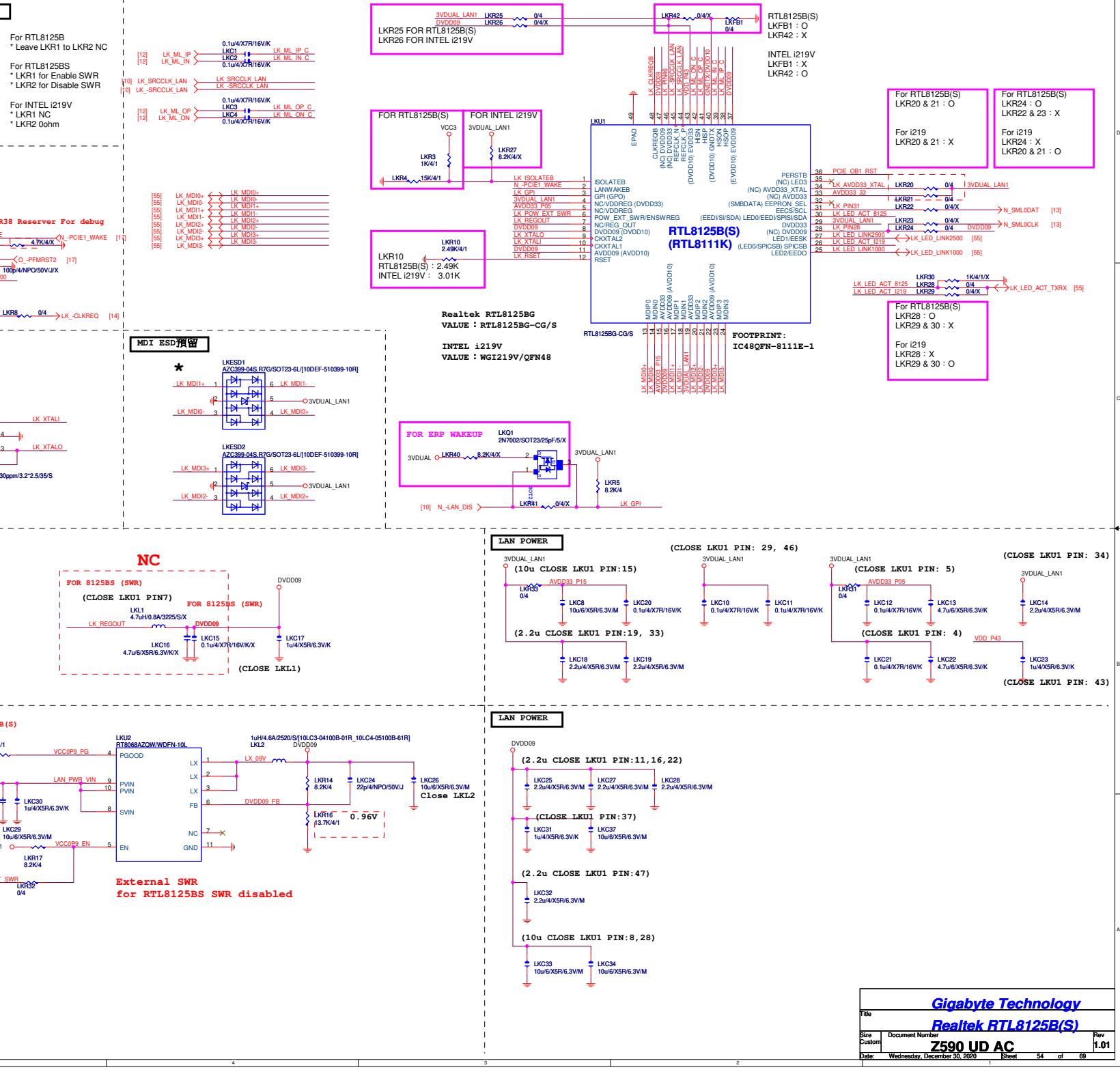
FOR 8125BS (SWR)

FOR 8125BS (SWR)

FOR 8125BS (SWR)

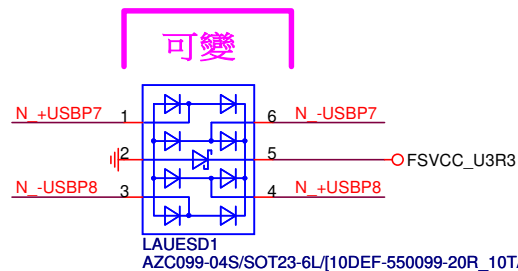
FOR 8125BS (SWR)

FOR 8125BS (SWR)



R0.3

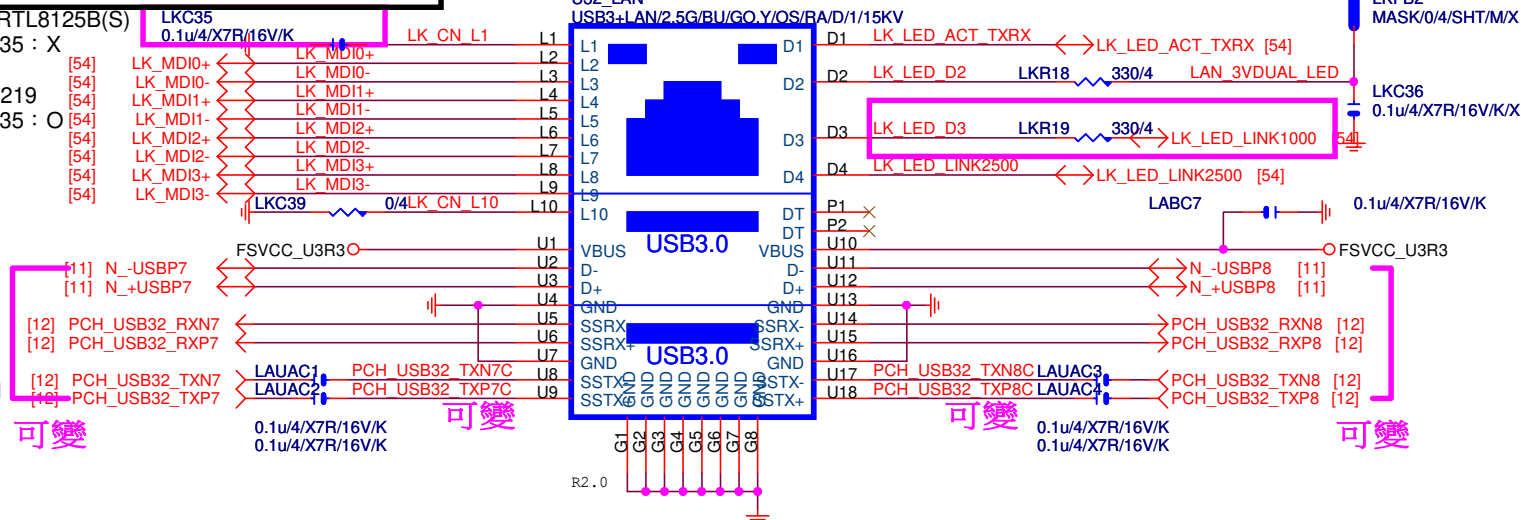
note:可變更USB NAME



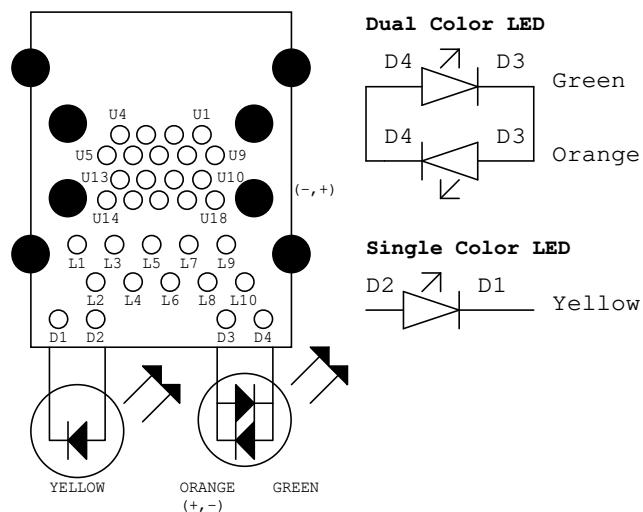
note:可變更USB NAME

LA_MDI-->100歐姆:[20/4/8/4/20]

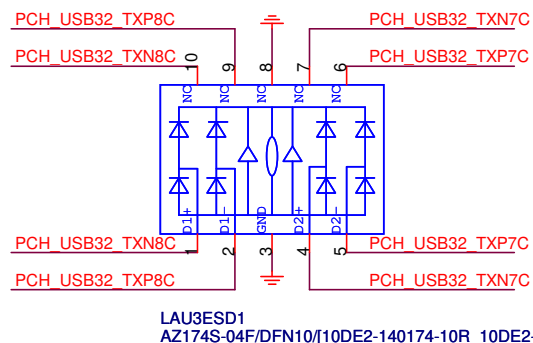
For RTL8125B(S)
LKC35 : X [54]
For i219 [54]
LKC35 : O [54]



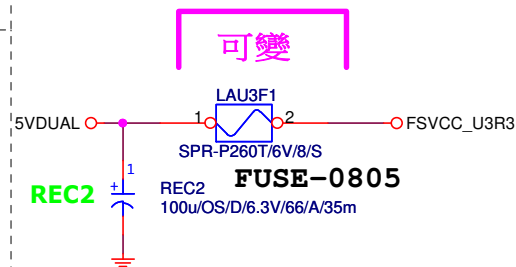
示意圖



note:可變更USB NAME



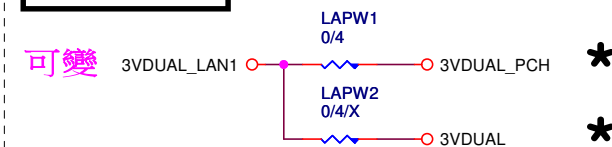
note:可變更FUSE



Close to connector

PS:視EMI需求

note: lan power連接及電流

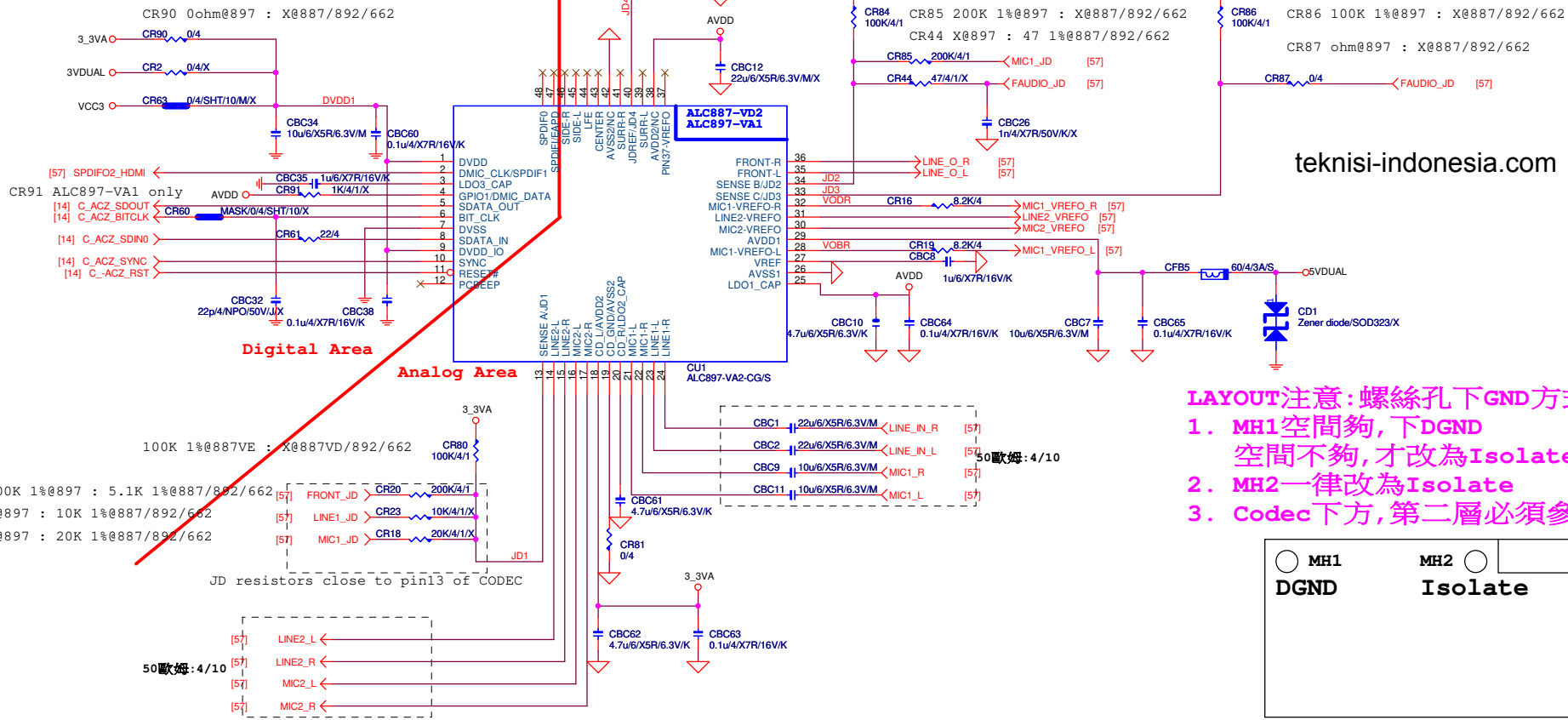


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LAN CONNECTOR-RTL8125B(S)

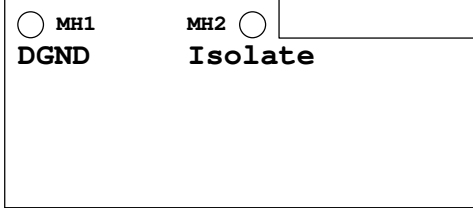
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LAYOUT注意:螺絲孔下GND方式
1. MH1空間夠,下DGND
空間不夠,才改為Isolate
2. MH2一律改為Isolate
3. Codec下方,第二層必須參考GND



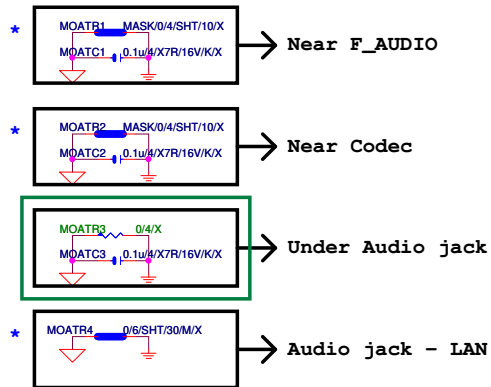
		897	887/892/662
Pin03	LDO3	1uF	10uF
Pin09	DVDD-IO	0.1uF	1uF
Pin18	AVDD2	4.7uF/0.1uF	NC
CR81	AVDD2	0ohm	NC
Pin20	LDO2	4.7uF	NC
Pin25	LDO1	4.7uF	22uF
CR83	LDO1	NC	0ohm
Pin27	VREF	1uF	10uF
Pin38	AVDD2	NC	22uF

BOM OPTION : 1. Chemicon音效電容
2. 金屬外罩 Reserve (LAYOUT上件與否,依照各Model spec)
3. LED Reserve (上件與否和LED顏色,依照各Model spec)

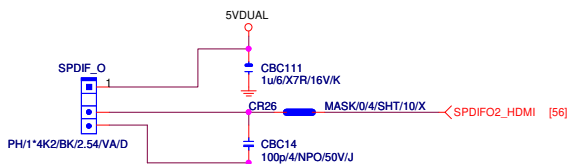
GIGABYTE™			
Title HD AUDIO ALC887VE/887VD			
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Pin20 LDO2

Rev 6.0

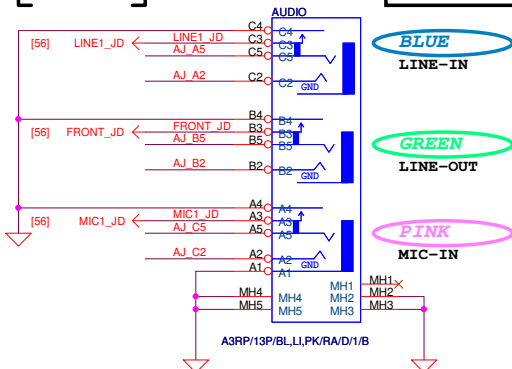
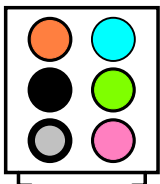


*量産前,MOATR1/MOATR2/MOATR40ohm改short pad

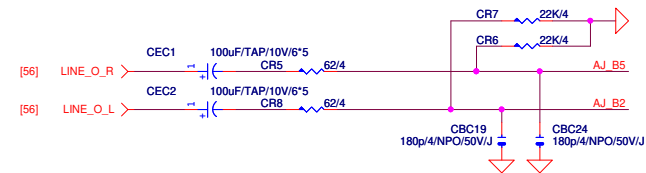


For HDMI SPDIF (依SPEC保留或移除)

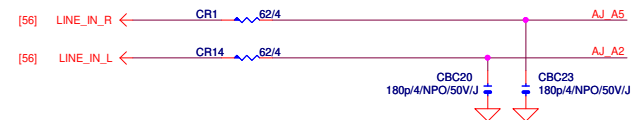
AZALIA JACK



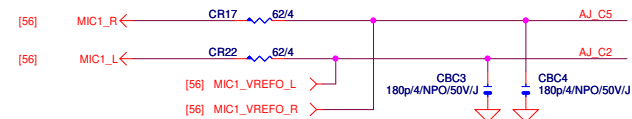
LINE-OUT



LINE-IN



MIC-IN

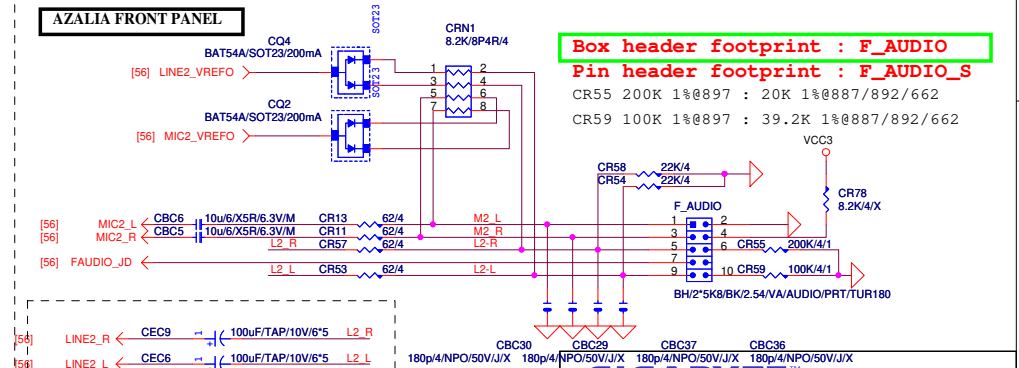


SURROUND

CEN/LFE

SURR BACK

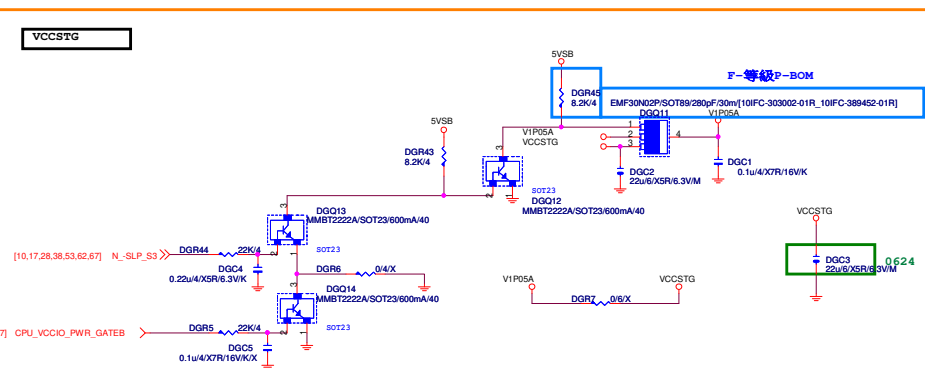
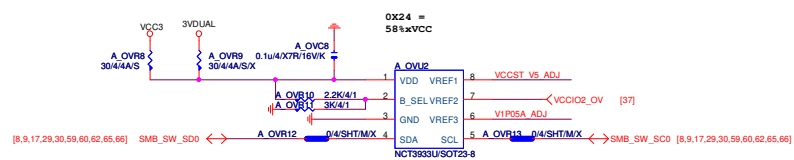
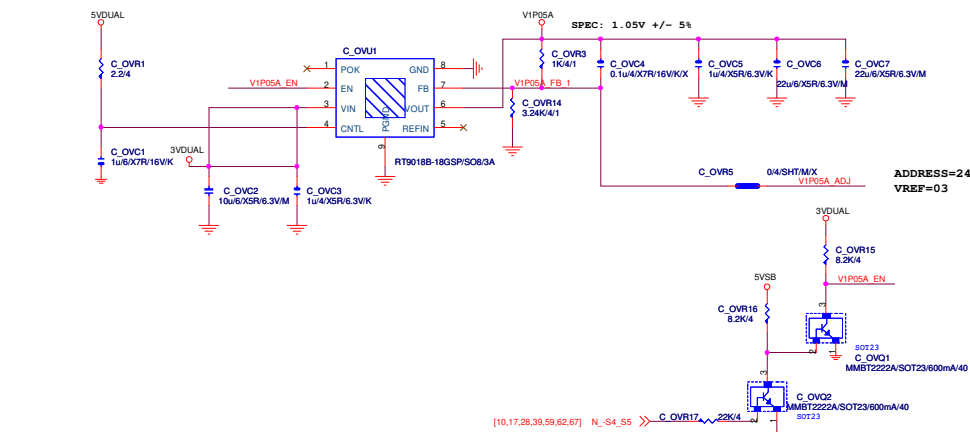
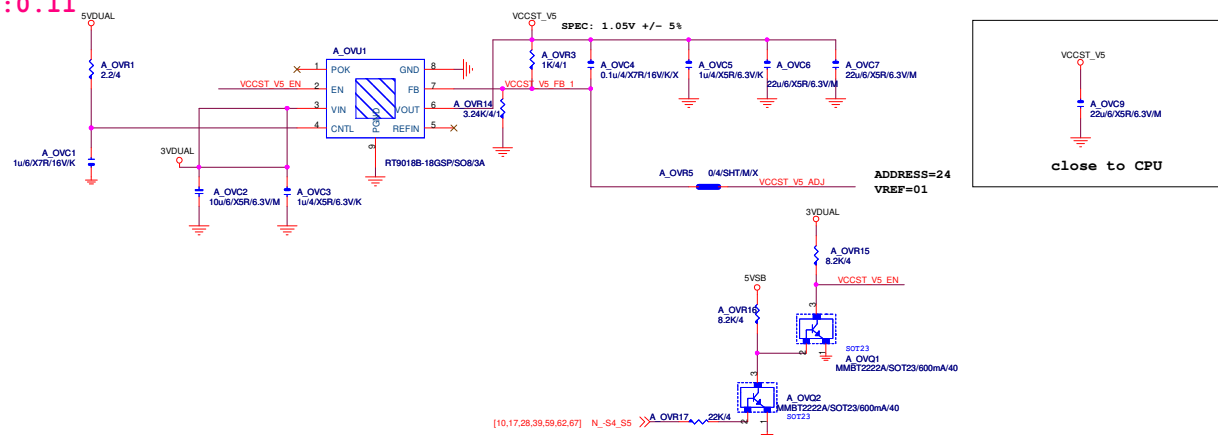
AZALIA FRONT PANEL



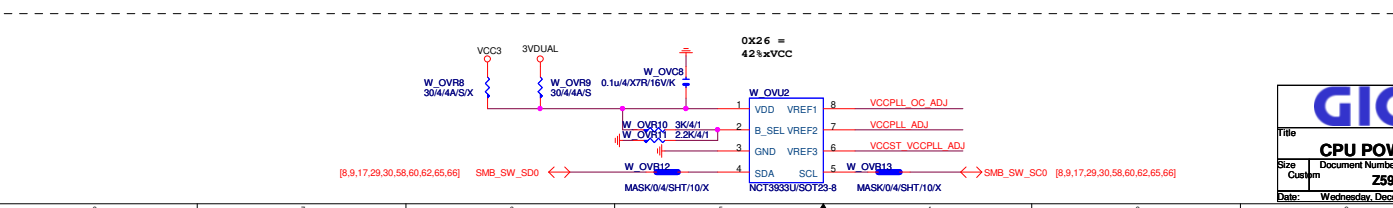
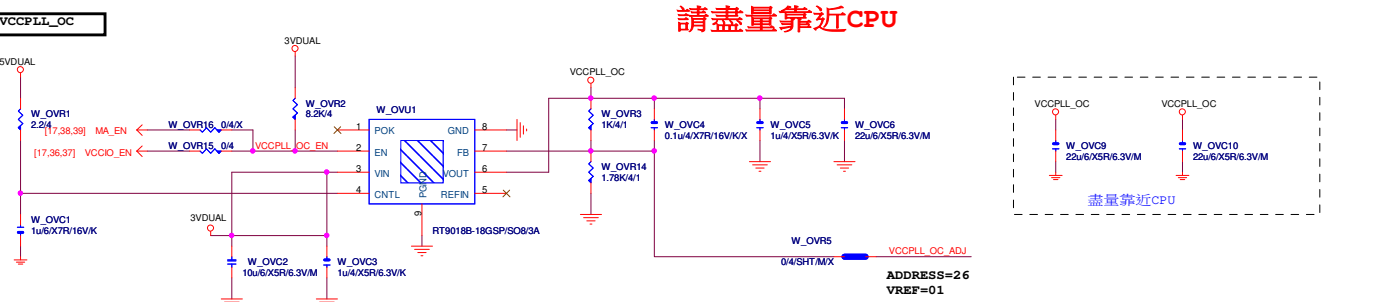
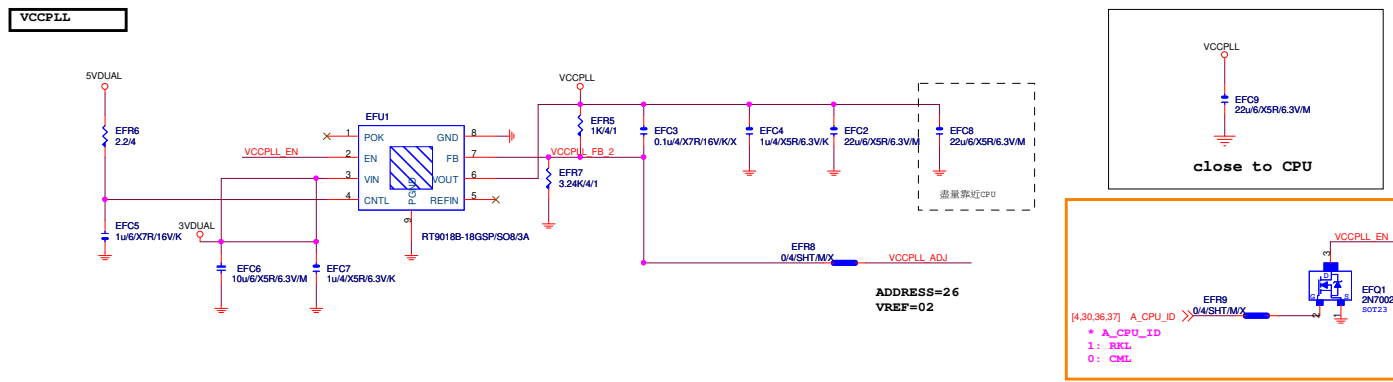
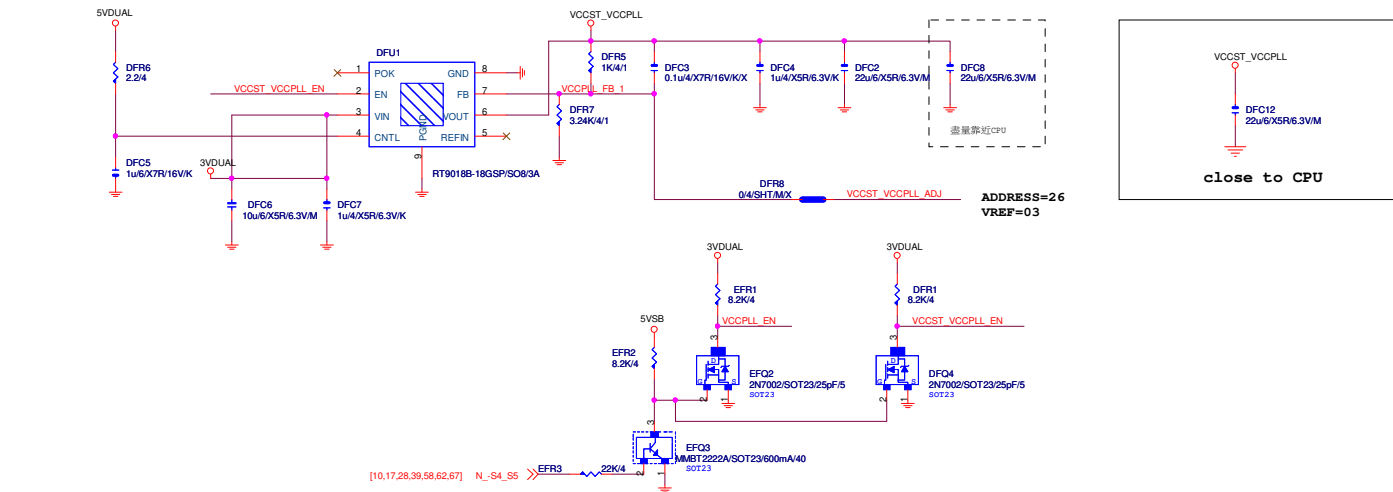
GIGABYTE

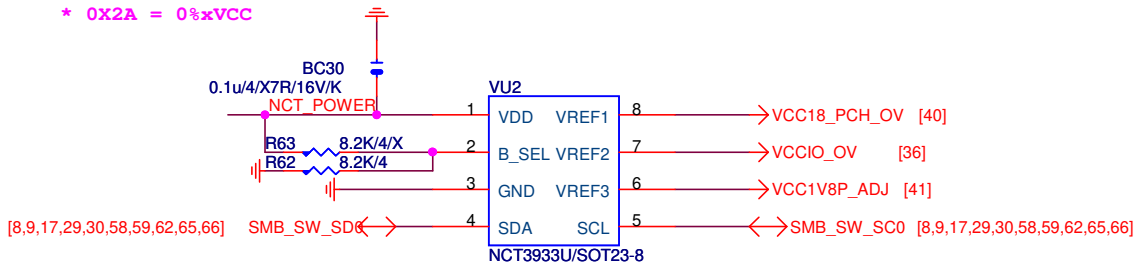
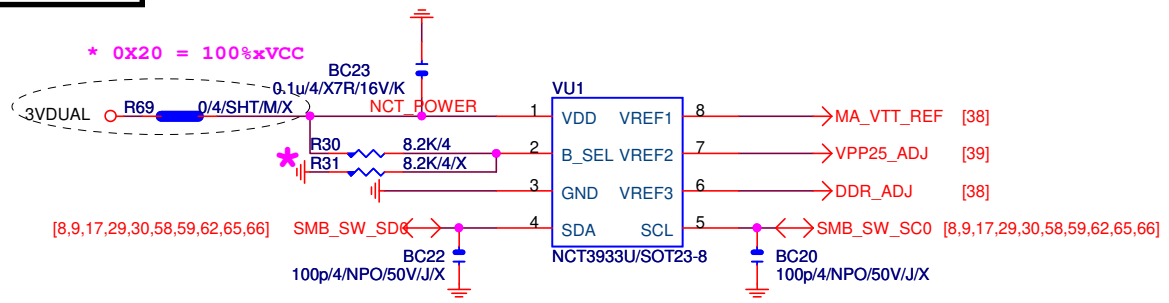
Title		
AUDIO JACK		
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REV:0.11



VCCST_VCCPLL 替換原先MOS開關線路





NCT3933	0X2A	0X20
VREF1	VCC18_PCH	DDRVTT
VREF2	VCCIO	VPP25V
VREF3	VCC1V8_PRIM	VDDQ

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CPU CORE VR-2

Size Custom

Document Number

Rev

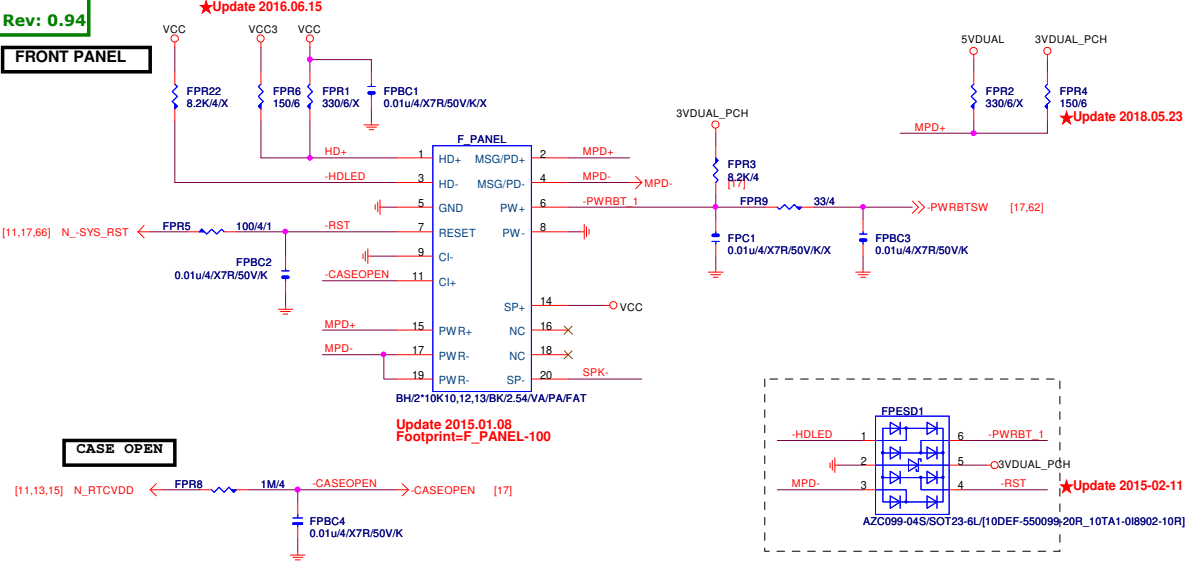
Wednesday, December 30, 2020

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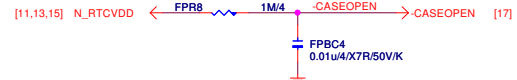
Z590 UD AC

1.01

FRONT PANEL

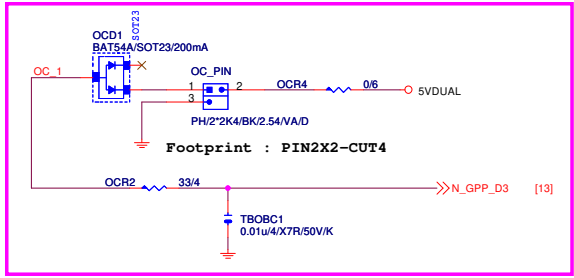


CASE OPEN

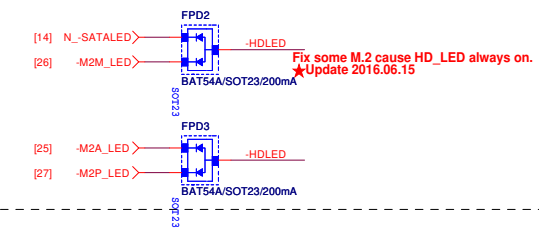


FRONT PANEL SHORT

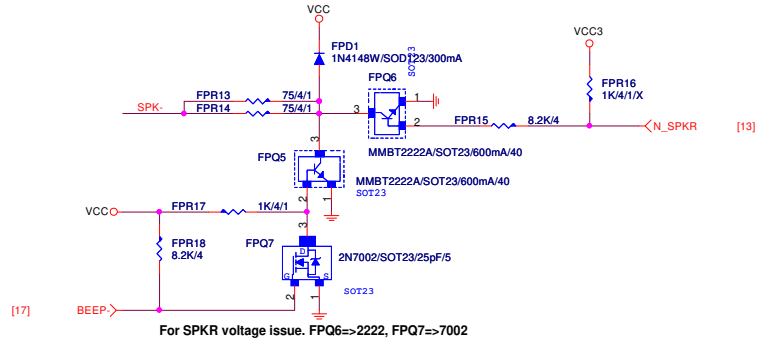
* FOR 客户Button



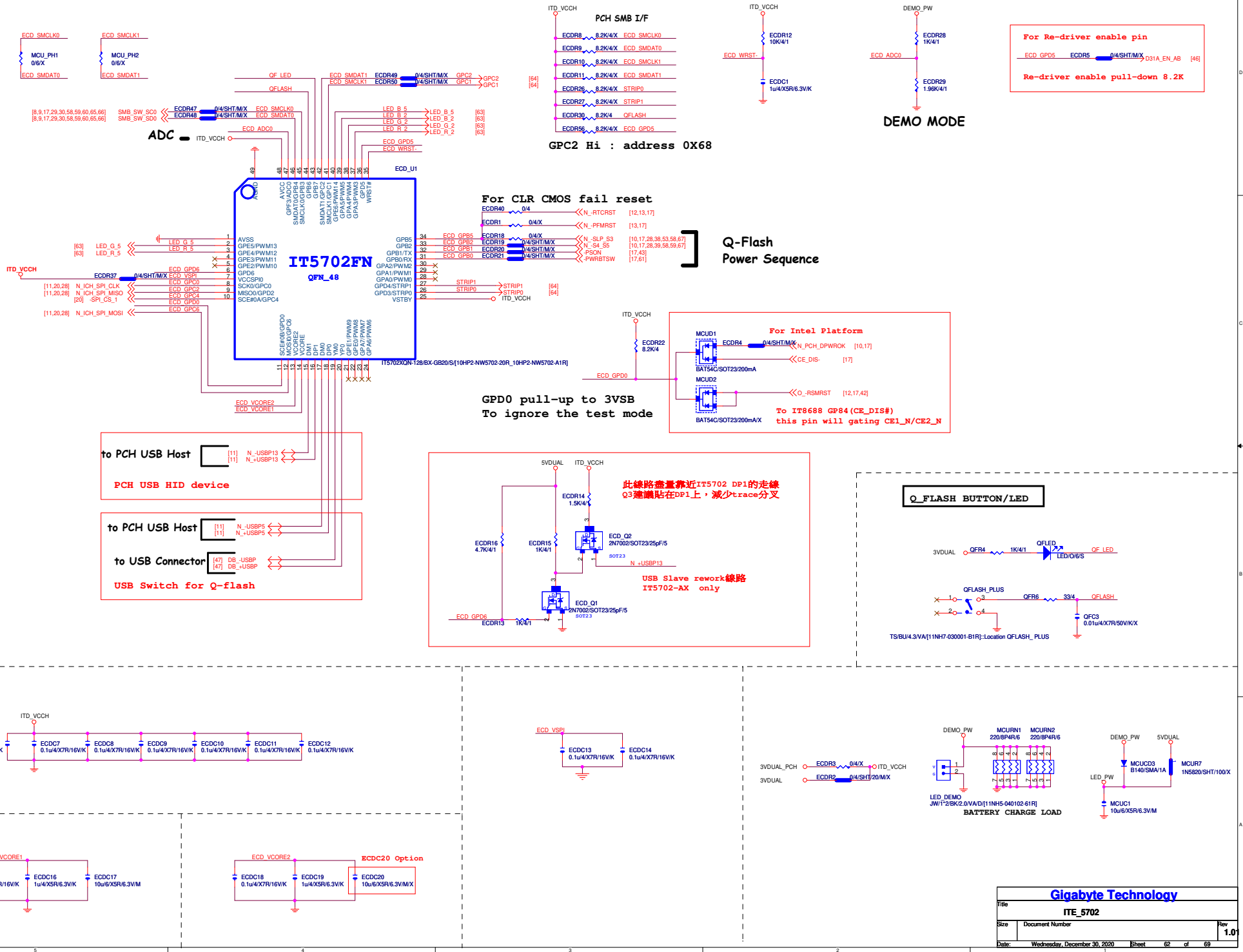
SATA/M.2 LED



SPKR W/O EC

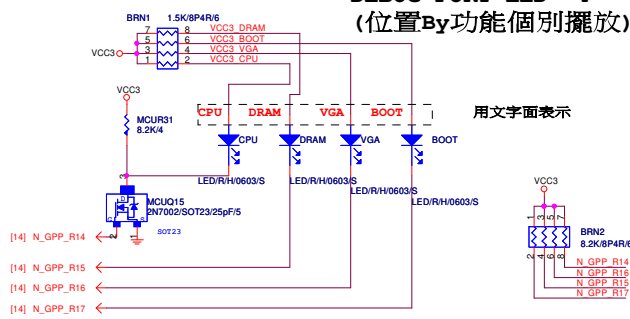


ECD_U1 請放在PCH到BIOS路徑上. 避免線過長



第一區 LED

DEBUG PORT LED *4
(位置By功能個別擺放)



N_GPP_R14	CPU DEBUG
N_GPP_R15	DDR DEBUG
N_GPP_R16	VGA DEBUG
N_GPP_R17	BOOT DEVICE DEBUG

第三區 LED

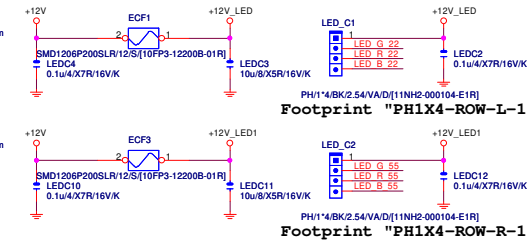
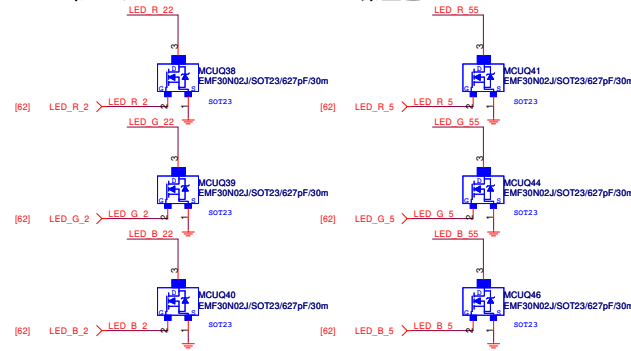
第五區 LED

第二區 LED CONTROL

第五區 LED CONTROL

燈條 LED (LED_C1放在PCB左邊板邊位置)

燈條 LED (LED_C2放在PCB右邊板邊位置)

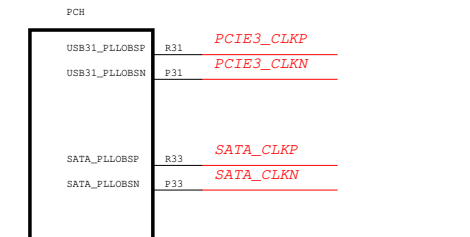
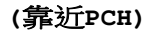


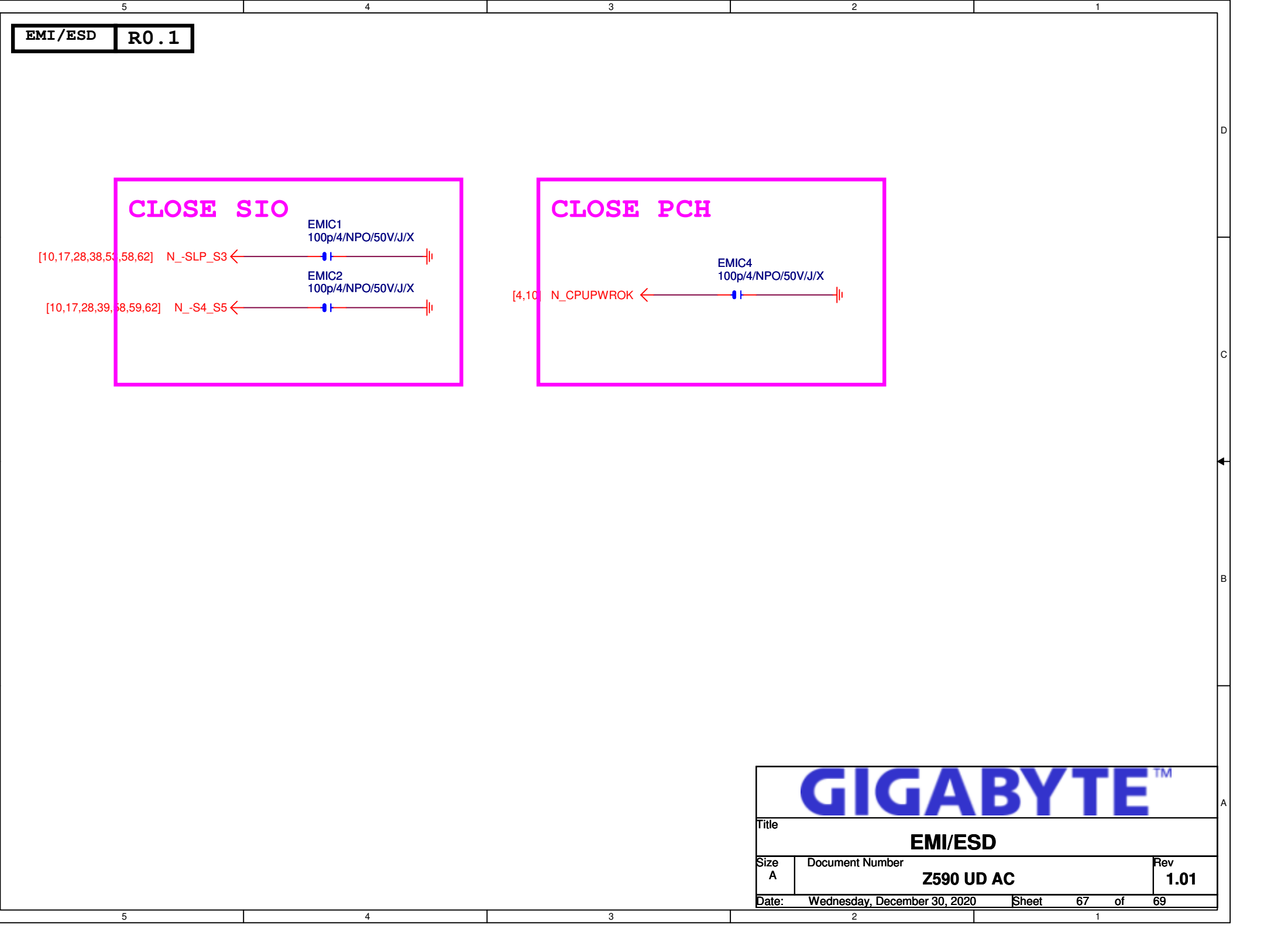
第四區 LED

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INTERNAL





POWER BLOCK MAP

```

graph LR
    subgraph CPU
        CPU_VCORE[VCORE]
        CPU_VCCGT[VCCGT]
        CPU_VCCSA[VCCSA]
        CPU_VCCIO[VCCIO]
        CPU_VCCIO2[VCCIO2]
        CPU_VCCST_VCCPLL[VCCST_VCCPLL]
        CPU_VCCPLL[VCCPLL]
        CPU_VCCPLL_OC[VCCPLL_OC]
        CPU_VCCST_V5[VCCST_V5]
        CPU_V1P05A[V1P05A]
        CPU_VCCSTG[VCCSTG]
        CPU_VDDQ[VDDQ]
    end

    subgraph DDR4
        DDR4_VDDQ[VDDQ]
        DDR4_DDRVTT[DDRVTT]
        DDR4_VPP_25V[VPP_25V]
    end

    subgraph PCH
        PCH_VCC18_PCH[VCC18_PCH]
        PCH_VCC1V8_PRIM[VCC1V8_PRIM]
        PCH_VCCPRM_1P05[VCCPRM_1P05]
        PCH_VCCDPHY_1P24[VCCDPHY_1P24]
        PCH_VCC0P85_PCH[VCC0P85_PCH]
        PCH_VCC3_PCH[VCC3_PCH]
        PCH_3VDUAL_PCH[3VDUAL_PCH]
        PCH_VCC3[VCC3]
        PCH_N_RTCVDD[N_RTCVDD]
    end

    subgraph IT8689
        IT8689_IT_VCCH[IT_VCCH]
        IT8689_IT_AVCC[IT_AVCC]
        IT8689_2_5LEVEL[2_5LEVEL]
    end

    subgraph HM
        HM_+12V[+12V]
        HM_VCC[VCC]
        HM_VCC3[VCC3]
        HM_VCORE[VCORE]
        HM_VCCGT_IMON_VCCGT[VCCGT (IMON_VCCGT)]
        HM_VDDQ[VDDQ]
        HM_VCCSA_IMON_VCORE[VCCSA (IMON_VCORE)]
    end
  
```

The diagram illustrates the power block map for the system, showing connections for various components:

- CPU:** VCORE, VCCGT, VCCSA, VCCIO, VCCIO2, VCCST_VCCPLL, VCCPLL, VCCPLL_OC, VCCST_V5, V1P05A, VCCSTG, VDDQ.
- DDR4:** VDDQ, DDRVTT, VPP_25V.
- PCH:** VCC18_PCH, VCC1V8_PRIM, VCCPRM_1P05, VCCDPHY_1P24, VCC0P85_PCH, VCC3_PCH, 3VDUAL_PCH, VCC3, N_RTCVDD.
- IT8689:** IT_VCCH, IT_AVCC, 2_5LEVEL.
- HM:** +12V, VCC, VCC3, VCORE, VCCGT (IMON_VCCGT), VDDQ, VCCSA (IMON_VCORE).

Figure 1-1 illustrates the pin configuration of the ISL69269-12+1 IC. The IC is shown as a large rectangle with the label 'ISL69269-12+1'. To the left of the IC is a box labeled 'V CORE/VCCGT'. To the right, under the heading 'DrMOS', are six pins labeled 'SIC651A'. The top five pins are connected to a common bus labeled '12相' (12 phases), which then connects to a terminal labeled 'V CORE'. The bottom pin is connected to a terminal labeled 'VCCGT'.

POWER

VCC ○

5VSB ○

S.W MOSFET

5VDUAL ○

L1085

3VDUAL ○

RT8120

VDDQ ○

NCT3103

DDRVTT ○

RT8068

VPP_25V ○

RT81269

VCC18_PCH ○

5VDUAL ○

RT9018

VCCST_V5 ○

RT9018

V1P05A ○

RT9018

VCCST_VCCPLL ○

RT9018

VCCPLL ○

RT9018

VCCPLL_OC ○

L1117

3VDUAL_PCH ○

FUSE POWER F/R

F_USB2
FSVCC_U2F2

F_USB1
FSVCC_U2F1

5VDUAL

AUDIO

U32_LAN

U32

U32G2

KB_MS_USB

FSVCC_U3R2

FSVCC_KM

FSVCC_U3R3

FSVCC_U3R1

FSVCC_U3F1

F_U32

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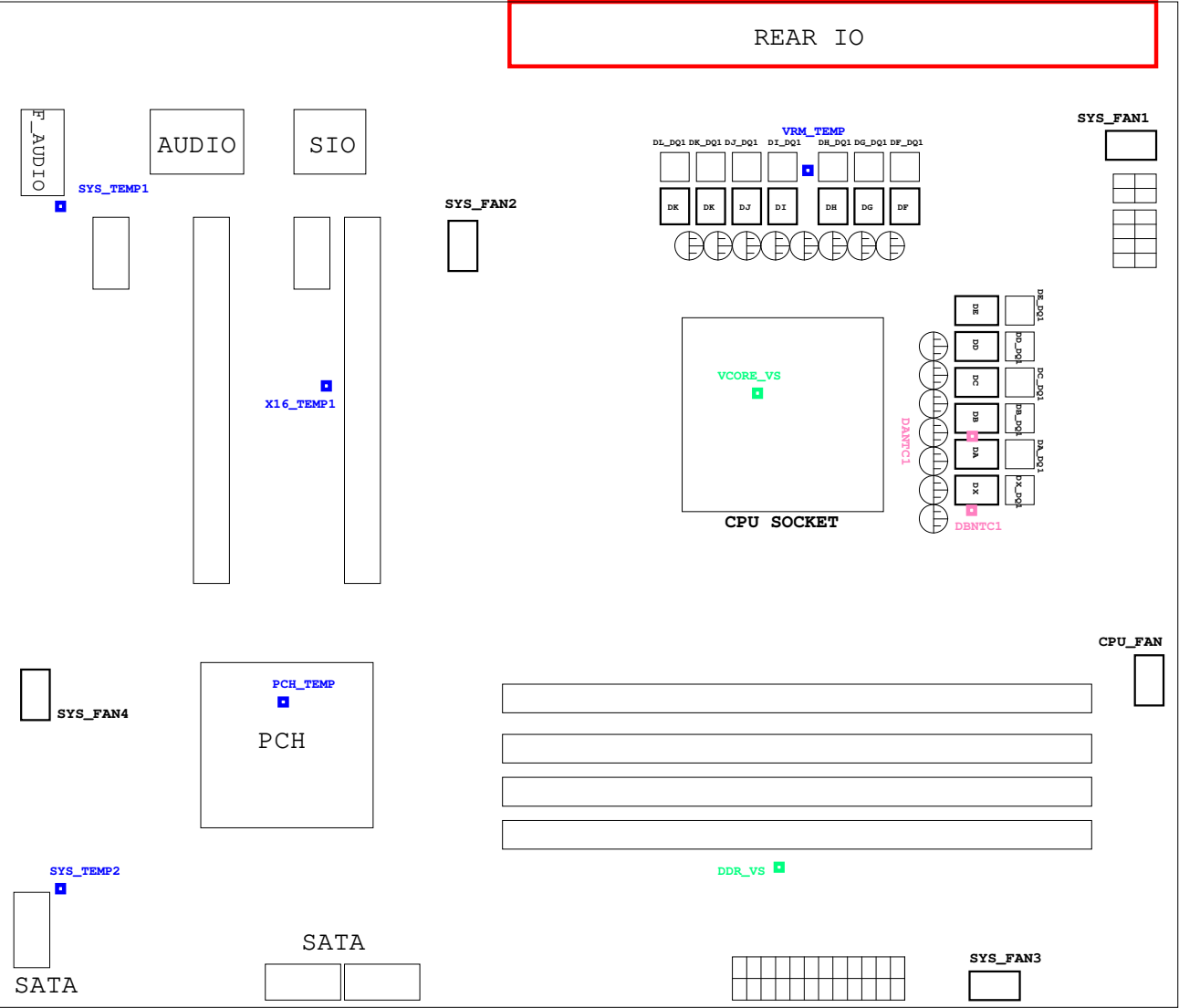
POWER MAP

Z590 UD AC

Size B Document Number 1.01

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熱敏電阻	擺放靠近位置	走線方式
DANTC1	DB_DL1	Differential
DBNTC1	DX_DL1	Differential
VRM_TEMP	DC_DQ1	N/A
X16_TEMP1	PCIEX16	N/A
PCH_TEMP	PCH	N/A
SYS_TEMP1	F_AUDIO	N/A
SYS_TEMP2	F_PANEL	N/A

- SIO RS
- PWM RS
- SIO VIN

■ FAN